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A REVIEW OF THE SEMICONDUCTOR STORAGE OF TELEVISION SIGNALS:

Part 2 — Applications 1975 - 1986

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Summary

This is the second of two Reports. In the first[1]*, the emerging semiconductor memory technology over the last two decades and some of the important operational characteristics of each ensuing generation of device are described together with the design philosophy for forming the devices into useful tools for the storage of television signals. This second Report describes some of the applications, as developed in BBC Research Department over the period 1975 - 1986. These include improved television synchronisers, high-quality PAL decoders, television noise reducers, film-dirt concealment equipment and buffer storage for television picture processing equipment such as stills stores. The continuing developments in the technology promise still further increases of memory capacity and there is a proposal to build a mass semiconductor television picture sequence store, initially as a research tool.*

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A REVIEW OF THE SEMICONDUCTOR STORAGE OF TELEVISION SIGNALS:

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1. INTRODUCTION

The first Report[1], and companion to this one, described how semiconductor memory technology developed from the earliest 64-bit devices into the megabit chips of today. Over this period the acceleration in memory density has been accompanied by improved performance in terms of speed of access and power consumption and also by falling unit costs in terms of price per bit of storage. The operational characteristics of dynamic semiconductor memory devices, in particular, have also adapted as the technological improvements made it possible. For example, the scaled metal-oxide-silicon (MOS) process and the introduction of substrate bias circuits made it possible to drive the chips from a single low voltage (5 V) power supply. Also the requirement to provide external memory refresh is made considerably easier by built-in 'hidden' refresh mechanisms which access rows of memory cells in strict rotation.

This Report examines in some detail the many and varied applications of semiconductor memory to television engineering. Some examples are taken from projects which were begun as research tools, such as providing field and picture-delay elements to assist with television synchronisers, noise reducers and film-dirt concealment equipment. Others focus on the bulk storage aspects, such as for buffer storage of television pictures and the construction of a mass television picture sequence store possessing many of the virtues of a digital video tape recorder.

2. EARLY DESIGNS

2.1 The 'Wardrobe' stores

The earliest random access store of any size at BBC Research Department[2] was that constructed from 1 Kbit shift registers in the mid-1970s before the simplest read-write memory devices became cost effective. The store was required to have a word capacity at least equivalent to the active area of one television picture, when sampled at the then common sampling standard of about 13.3 MHz which is 3 f_{sc}.* An active picture then comprised 576 lines of 692 samples and each sample was to be 8 bits. The maximum data transfer rate had to exceed 13.3 Mword/s. To meet the requirements of a large variety of applications, it was necessary to incorporate a wide range of facilities in the final design. The operation and control of the store also had to be largely self-contained in order to avoid the need for different user groups to design and construct complex store-control equipment. This feature made the use of the store by such groups relatively economical, as each group had only to concentrate on the problems peculiar to its own work and not on the internal design of the store.

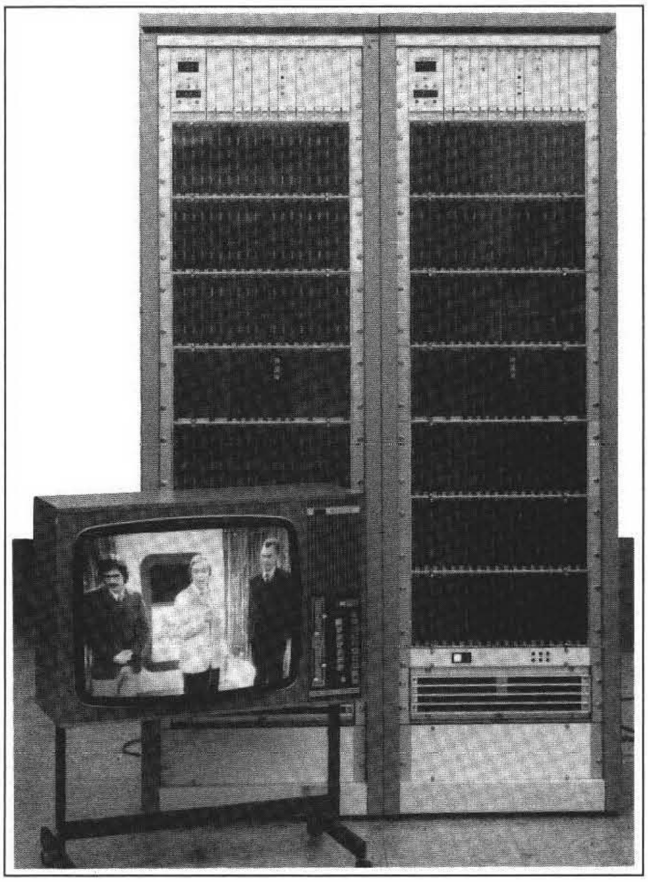

Fig. 1 - The 1975 picture store.

The store was constructed in two autonomous halves so that two different groups could each use one half, that is one field (288 lines) of storage. The inputs and outputs were asynchronous, and any line of data stored was randomly accessible. Two independent 'read' outputs were available from each half of the store making a total of four outputs when the two halves were used together. This arrangement was convenient for work such as standards conversion where interpolation between several lines is necessary.

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* where f_{sc} is the System I PAL colour subcarrier frequency.

There were four additional requirements imposed on the design. The stores were to be transportable, incorporate a comprehensive self-checking arrangement, operate at lower sampling frequencies than the maximum and perform statically although employing 'dynamic' devices.

The stores as constructed are shown in Fig. 1, displaying their single picture. Each field store consumes about 1 kW!

2.2 Experiments with early read-write memories

A number of experiments were made following the construction of the stores just described to study the use of the emerging read-write memory devices. The major advantage over shift registers to be gained in constructing a memory store from such devices is the flexibility of write-in and read-out addressing. Read-write memories of 1 Kbit capacity were available constructed from both bipolar (TTL, ECL) and static MOS technology. The bipolar products were fast ($\approx$100 ns cycle time) but they had very high dissipation ($\approx$1 mW/bit) and they were expensive. MOS devices, on the other hand, were relatively cheap, with a lower power dissipation ($\approx$0.2 mW/bit) but they suffered from a slow cycle time ($\approx$300 ns). At digital video sampling rates of 13.3 MHz a convenient demultiplex factor for these latter devices was found to be sixteen giving a store cycle time of 1.2 μs and allowing two opportunities to access the store at video rate. If the devices which stored just 1 bit per address were chosen a minimum number of 128 (8 x 16) devices would have been necessary for an 8-bit video signal giving a total minimum capacity of 16 Kbytes or about twenty television lines. To reduce the package count for a small experimental store a device with parallel storage of several bits at each address was preferred and one device with an organisation of 256 x 4 bits was produced by several manufacturers. The necessary demultiplex factor of 16 required 32 of these, providing storage of more than four television lines. One manufacturer, AMD, produced the fastest version of this device and its timing requirements were less demanding than some of the others. A small store was therefore constructed using 32 devices to test the feasibility of the techniques proposed and the results were encouraging.

When the 4 K x 1 devices first became available they were dynamic and required thought to be given to arranging for their periodic refresh. They were, however, lower in power dissipation and, for the same store cycle time proposed earlier, the minimum size of store possible with these devices was about 77 television lines. A printed-circuit board (p.c.b.) design was eventually produced, containing thirty-two devices and this was capable of holding a quarter of a television field, 4 bits wide on a single 4U BMM p.c.b.*. It was supplied with three different d.c. voltages (+5 V, +12 V and −5 V) and incorporated special circuitry to ensure that the substrate voltage (−5 V) was supplied before the others and removed after them. A television picture store was constructed using sixteen of these boards and controlled by a special logic board which was intended to provide flexible store control for different potential users. Several units were built and used for early work on standards conversion[3] for which the four independent outputs were essential.

2.3 A digital field-delay using 64 K CCDs†

During 1978 a digital field delay was required for a video noise reduction application[4]. A charge-coupled device (the CCD 464), capable of storing 64 Kbit data became available from Fairchild. By considering the active field period only the storage can be accommodated in thirty-two 64 K devices, which gives a convenient organisation, for an 8-bit signal, of four 64 K stores for each bitstream. These can be assembled on a single 4U board and such an economy of space was thought to be well worth achieving. In fact, the development was somewhat speculative as, at the time, the devices were not being manufactured in volume and those used were pre-production samples. However, in other respects they appeared to be ideally suited to the application since their shift register organisation, with low power consumption was exactly what was needed.

The maximum clocking frequency of the device was quoted as 4 MHz. This implied a four-way demultiplex at the chosen sampling frequency, giving 32 parallel bit streams, one device per stream. As a result, serial-to-parallel and parallel-to-serial converters operating on the input and output data, respectively, were required. The charge-coupled device itself, is organised as a serial-parallel-serial structure with 16 parallel registers, each of capacity 4 Kbits. Data is stored by filling each register successively, using a four-bit address to determine which register is used at any instant.

Data is shifted in all 16 registers simultaneously on receipt of clocks and reading takes place at the same location as writing. The complex clocking arrangements meant that the 32 storage devices required an overhead of 27 ancillary devices. Nevertheless, it proved feasible to mount all the components on a single 4U board with a power consumption of about 14 W. A general view of the board is shown in Fig.2.

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* A binary-metric-modular racking system (BMM) based on a standard rack width and heights in units of 1 U which is approximately 45 mm high. A 4 U BMM p.c.b. measures approximately 156 mm x 256 mm.

† The picture store was designed and commissioned by A. Oliphant.

The clock waveforms and addresses for both field store boards are generated on a separate housekeeping board. Trimming of the data delay is accomplished by omitting clock pulses during the line blanking interval and, for NTSC operation, which requires significantly less storage than PAL, omitting CCD addresses. These operations are again performed on the housekeeping board.

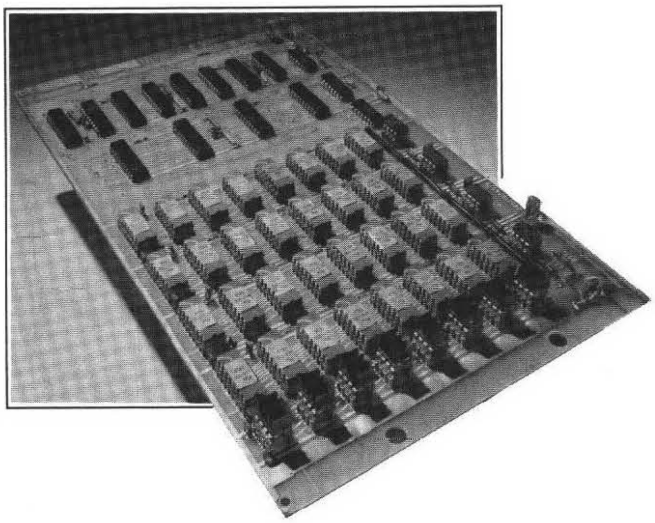

Fig. 2 - General view of the compact field store board based on 64 K CCDs.

In operation, the store was found to be fairly reliable but several CCDs failed in the course of two or three years and had to be replaced. Eventually, it became impossible to obtain further devices and failed devices were allocated to least significant bits of the store where their isolated errors would cause least damage.

3. THE 16 K GENERATION

3.1 An experimental 4 f_{sc} picture store

3.1.1 Introduction

This Section describes the design principles and construction of an experimental digital television picture store which was developed in early 1979 for work on television synchronisers and PAL decoding experiments at data rates up to 4 x f_{sc} — it is illustrated in Fig. 3.

At this time one contender for a standard video data sampling rate was based on $4f_{sc}$ ($\approx$18 MHz) and this store is capable of operating at this rate. The 1975 digital picture store based on shift registers and described in Section 2.1 was adequate for many applications but suffered from a long access time (more than four television lines). A more recent television field store based on 4 Kbit dynamic read-write memory devices (referred to in Section 2.2) and occupying about one quarter of the volume of the 1975 store was not capable of operating at 18 MHz. The introduction of 16 Kbit dynamic memory devices made it worth considering the development of a new television picture store for experimental purposes. The solution adopted was to use the existing 4 K-based store board design with a modified control board and replace the 4 K devices directly with 16 K devices. The mechanical arrangement of the 4 K-based store, however, contained many hand-wired looms which made the construction time-consuming. A speedier solution was achieved by redesigning the control circuits to operate at the faster rate and building these on conventional 4U BMM boards with a printed-circuit mother-board. The resulting picture store consists of a total of 12 p.c.bs which together with power supplies fits into the same case as the 4 K-based field stores (0.5 m x 0.5 m x 0.44 m) with room to spare — and the new picture store is illustrated in Fig. 3. The total cost at 1979 prices was about £3,000 and the total power consumption is 225 W. Television data is stored on a line-by-line basis where each line is identified by a LINE LABEL (10-bit) and the beginning of a line by a LINE TRIGGER and these together with a data output clock are supplied by the user. An asynchronous buffer allows data to be written into the store at a rate which is different from that at which it is read out. The buffer is made of sufficient capacity (48 samples in this case) to allow the delay of data through the entire store to be continuously variable provided the input and output clock frequencies are within ±0.1%.

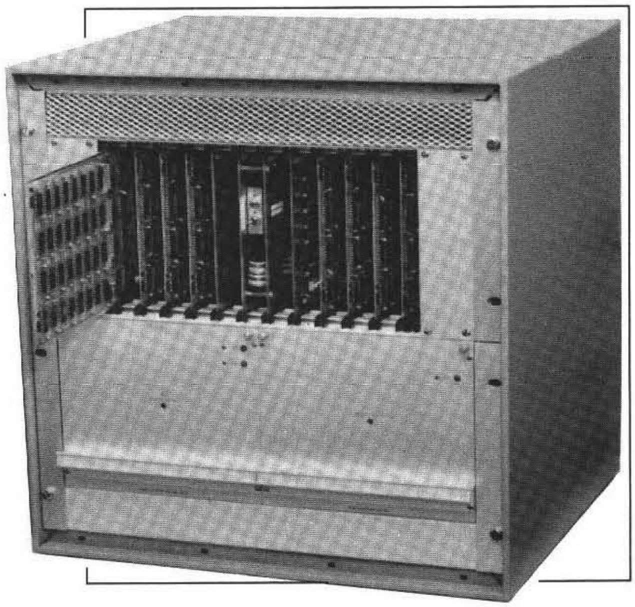

Fig. 3 - An experimental 4 f_{sc} picture store based on 16 K dynamic memory devices (1979).

The picture store is built as two separate field stores sharing a common control system. Each field store — see Fig. 4 — is divided into two halves, A and B, so that bunches of F samples of data can be written into A while F samples are read from B and vice-versa. Data is output from A and B via tri-state buffers which are enabled alternately every F sample periods to form one continuous stream of serial output data. In the main part of the store the write and read operations are synchronous with the clock rate of the output data and the delay is variable in steps of 16 output clock periods.

The initial asynchronous buffer is required to serve two functions. The overall store delay is quantised in steps of $2F$ samples — the length of the store cycle. A buffer, of minimum capacity $2F$ samples can, therefore, make the overall delay variable in discrete single sample steps. Further, for the buffer to be made asynchronous, (i.e. the clock rates associated with data into and out of the buffer are allowed to be different), the overall picture store delay can be made continuously variable up to a maximum of one television picture period. For asynchronous operation data is applied at an input data rate and removed at another clock rate which is user supplied and subsequently used to synchronise the main store operation.

3.1.2 Store board organisation

A block diagram of the storage arrangement for one of the four bits, on the store board designed originally for 4 Kbit devices and for operation at a higher frequency, is shown in Fig. 5. The board holds 32 devices (type 4116-3) each arranged as four parallel 1-bit data stores with a demultiplex factor of eight. Two of these boards are required to make up the 8-bit total required in each field block A or B. Taking the worst-case memory cycle time of 375 ns and the period between data samples as 55 ns, the minimum demultiplexing factor possible is 375/55 which is about 7. The maximum value of F which can be used depends on the total number of samples which each half of a field store, A or B, is required to hold. At a 4 x f_{sc} sampling rate the total number of samples generated each half-field[1] is 180,000. These can only be accommodated in 11 devices per bit: no multiplexing beyond 11 is, therefore, possible without under-using the available capacity of the memory

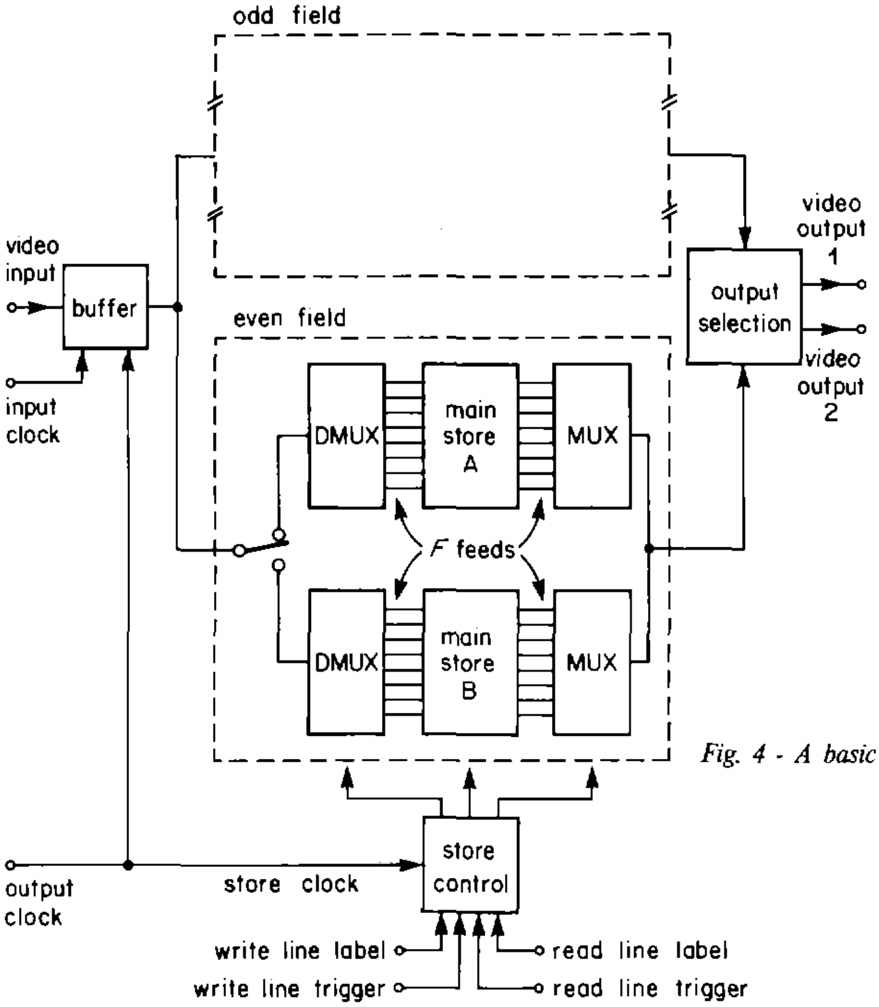

Fig. 4 - A basic schematic of the experimental 4 f_{sc} picture store.

devices. A summary of the number of samples stored for values of F between 8 and 11 is given in Table 1 where the cases (a) to (c) are defined as:-

a) all samples generated at 4 x f_{sc}
b) all samples generated at 4 x f_{sc} excluding field blanking
c) all samples generated at 4 x f_{sc} excluding field and line blanking.

With a demultiplex factor of eight the total store capacity is equivalent to about 99% of a 4 x f_{sc} sampled picture excluding both field and line blanking.

Table 1
The number of samples stored for different F

Demultiplex factor *F*	Total no. of devices for picture store	No. of samples stored in field block A or B	% samples stored		
			(a)	(b)	(c)
8	256	131,000	73	79	99
9	288	147,000	82	89	111
10	320	163,000	91	99	123
11	352	180,000	100	—	—

3.1.3 Store control

The main waveforms associated with the memory control signals required for both A and B sections of the field stores over a complete store cycle are shown in Fig. 6: all are generated synchronously from a counter whose successive clock periods are numbered 0 to 15. Consider the operation of a read cycle in the A section of the store. A read address, A_m, is set up during counts 1 to 8; the row part of the address occurring in the first half of this period (1 to 4) and the column part of the address in the second half (5 to 8). (The same address, A_m, is used to read from the other half of the store, B, during counts 9 to 0). The negative-going edges of the RAS and CAS waveforms latch the row and column parts of the address respectively into the memory devices. Because the WRITE A waveform is in the 'high' state after this time a read cycle is initiated and the data associated with the addressed memory locations are available after the appropriate access time which is approximately during counts 9 to 10 as shown. The LOAD pulse at count 9 loads eight data bits at a time into parallel-to-serial shift registers and the data exits

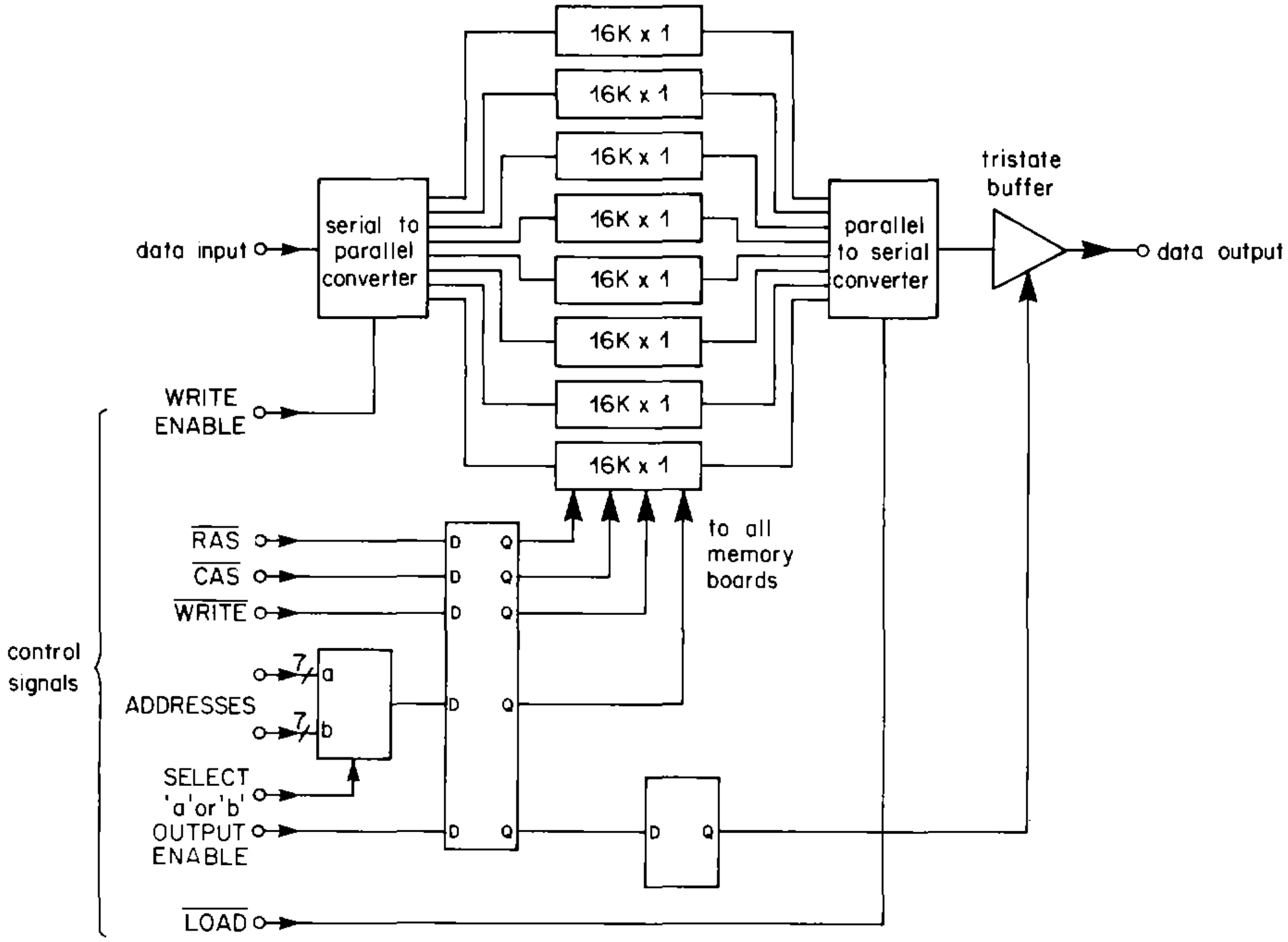

Fig. 5 - Block diagram of one-quarter of a store board which handles one bit of storage in one-half of a field.

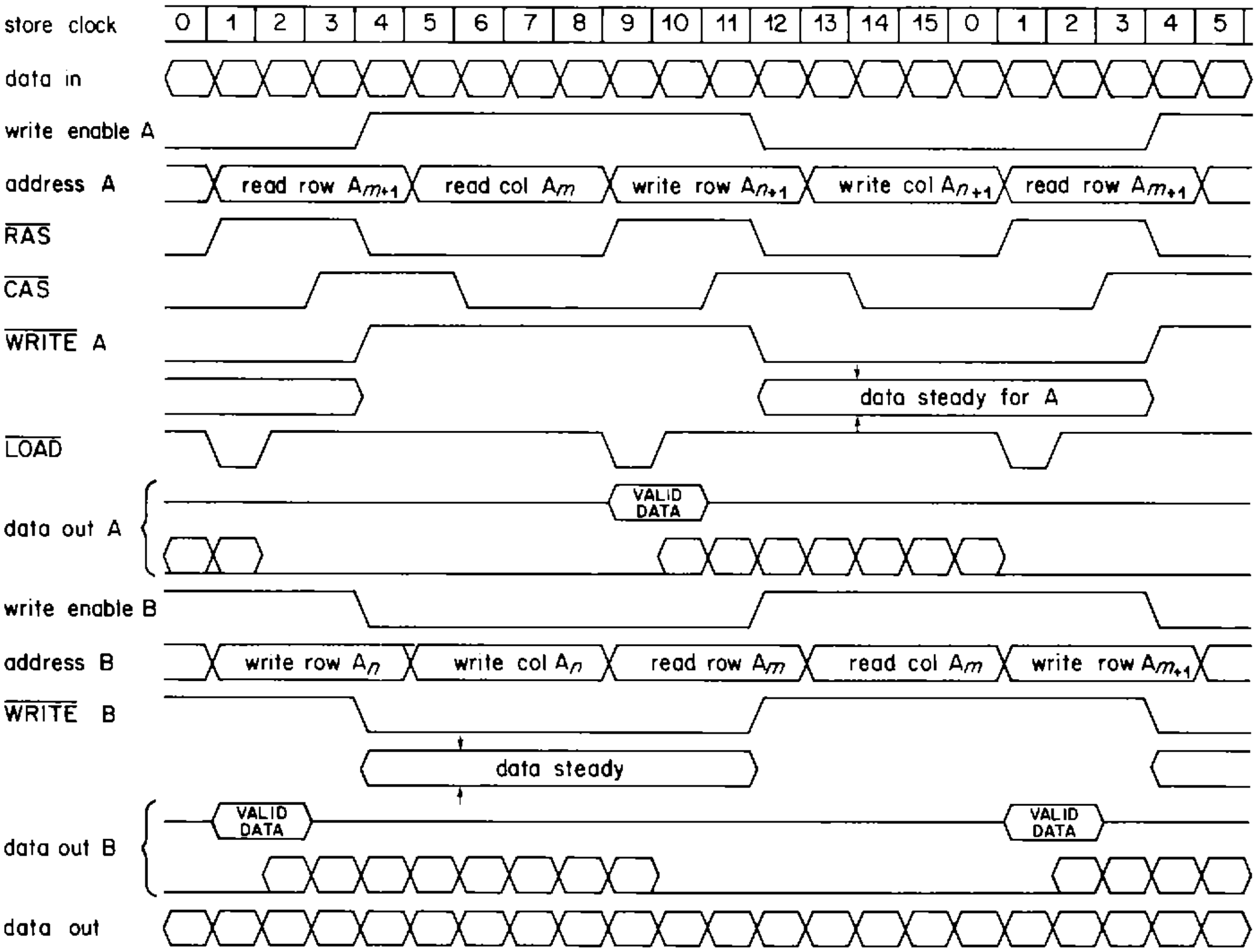

Fig. 6 - The store board control waveforms.

serially from the store during counts 10 to 1. An identical series of operations occurs for the B section of the store 8 clock periods later.

Next consider the operation of a write cycle in the A section of the store. Serial data is input to the store boards during count 4 to 11 and fed into serial-to-parallel converters so that during the period 12 to 3 the parallel data is held steady for writing into the memory devices. A write address A_{n+1} is set up during count 9 to 0; the row part on counts 9 to 12 and the column part on counts 13 to 0. (The same address is used to write into the other half of the store B during counts 1 to 8). The address is latched into the memories in the same manner as before but because the WRITE A signal is now in a 'low' state the available data is written into the memory devices.

In general the main store clock frequency gives rise to a non-integer number of store cycles over a television line period and arrangements are made for the last memory cycle in a line to be completed whilst at the same time re-synchronising the start of a new memory cycle to the next line trigger.

3.2 'Eric' based store

3.2.1 Introduction

By the end of the 1970s a new factor had appeared in the application of television picture stores. This was the increasing availability of microcomputers which lifted the use of picture storage into a new dimension. Now it was possible to communicate interactively with the stored video data, albeit at a slow rate ($\approx$1 Mbit/s), and process it in some way. The development of an Electronic Graphics generator produced a new picture store design which combined on a single p.c.b. the semiconductor storage, video multiplexing arrangements and an independent slow-rate data access port to connect it to a microprocessor, for a single data bit. The store board operated in conjunction with an original 8085 microprocessor bus design which became referred to as 'Eric'.* The store design was later adapted for an Enhanced Teletext equipment[5] which required 24 bits for each picture sample and allocated as 8 bits each for the red (*R*), green (*G*), and blue (*B*) components. A video data sampling rate of 13.5 MHz was chosen for the System I television standard which anticipated the proposed International Standard[6] for digital interfaces in studios. The 'active' picture area contains 720 x 576 pixel locations making for a minimum picture store capacity of just over 1.2 Mbytes (one byte is equivalent to 8 bits).

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* N.E. Tanton was responsible for this work.

The new picture store design contained thirty-two 16 K x 1 read-write memory devices which is sufficient to hold 512 K samples, and represents 25% more capacity than is required for one video component. Three such stores with eight bit-planes each are, therefore, required to hold the *R*, *G*, *B* samples and the extra capacity is used as auxiliary storage accessible by the computer port only.

Each group of eight bit-plane boards is interfaced to the microcomputer bus through control circuitry arranged as shown in Fig. 7. The block which connects directly to the computer bus (the X-Y controller) allows the picture store to be addressed asynchronously at the operating rate of the microcomputer by supplying two 10-bit numbers which identify a particular horizontal offset (*X*) and vertical offset (*Y*) and define *X*, *Y* coordinates of a displayed pixel. Slow-rate video data can be written to or read from the store via the computer data port independently of the full-rate video port; access to data and video ports is arranged to alternate approximately every microsecond. The store can also be used simply as an extension to the computer memory, in which case a single 19-bit address is used and data can be retrieved within about 2 μs. The timing of control signals and address generation is handled on the store control board which, in common with the other two picture stores, receives 13.5 MHz clock pulses and video synchronisation pulses from a common clock-pulse generator board.

In the design there is only one full-rate video port which is shared for video input and output. Video output generally takes precedence but single frames of video can be 'grabbed' into the store by momentarily interrupting the video output for two television field periods. Each video input port requires its own analogue-to-digital converter (a.d.c.) and video outputs are taken to their respective digital-to-analogue converters (d.a.c.) through additional boards which also interface with the microcomputer bus. These boards contain an array of small read-write memories which can be programmed to allow simple video post-processing such as picture blanking or gamma correction. The store is contained in an 8U BMM rack together with the associated a.d.cs and d.a.cs and is shown in Fig. 8. The three *X*-*Y* controller functions are housed in a separate microcomputer rack. The complete *R*, *G*, *B* store dissipates about 250 W.

3.2.2 Store board organisation

With the lower video sampling frequency of 13.5 MHz the minimum *F* is reduced to about five and for a total of 32 devices the maximum *F* could be made 32. A value of 16 was chosen as a compromise

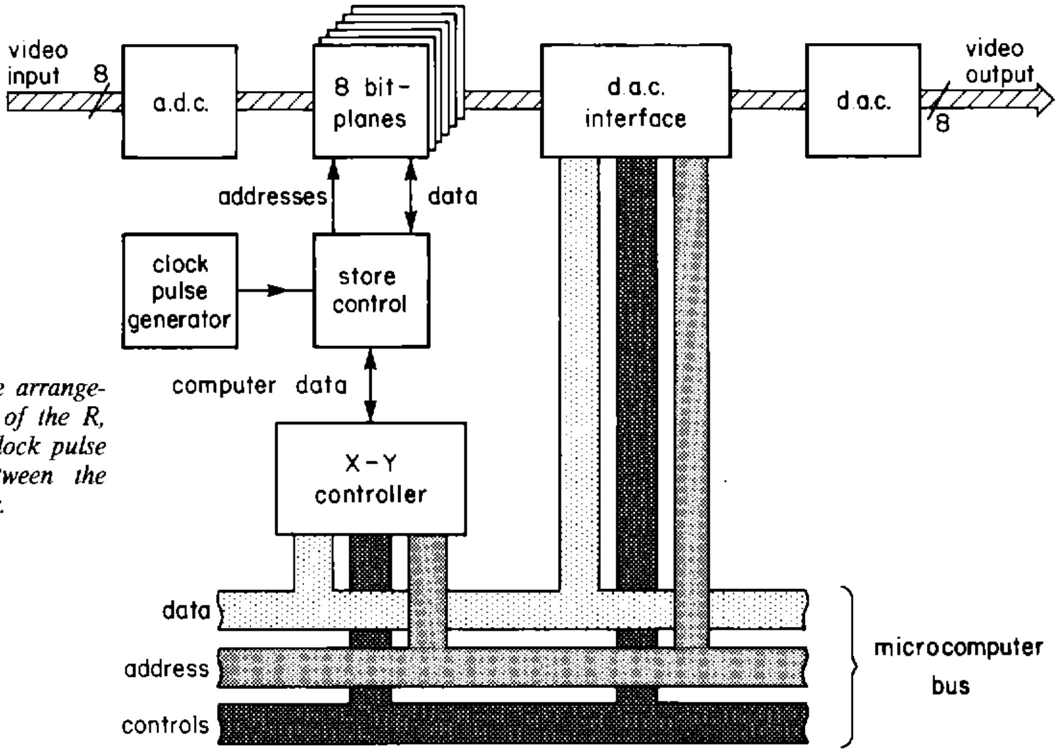

Fig. 7 - The picture store arrangement for one component of the R, G, B store (1981). The clock pulse generator is shared between the three components.

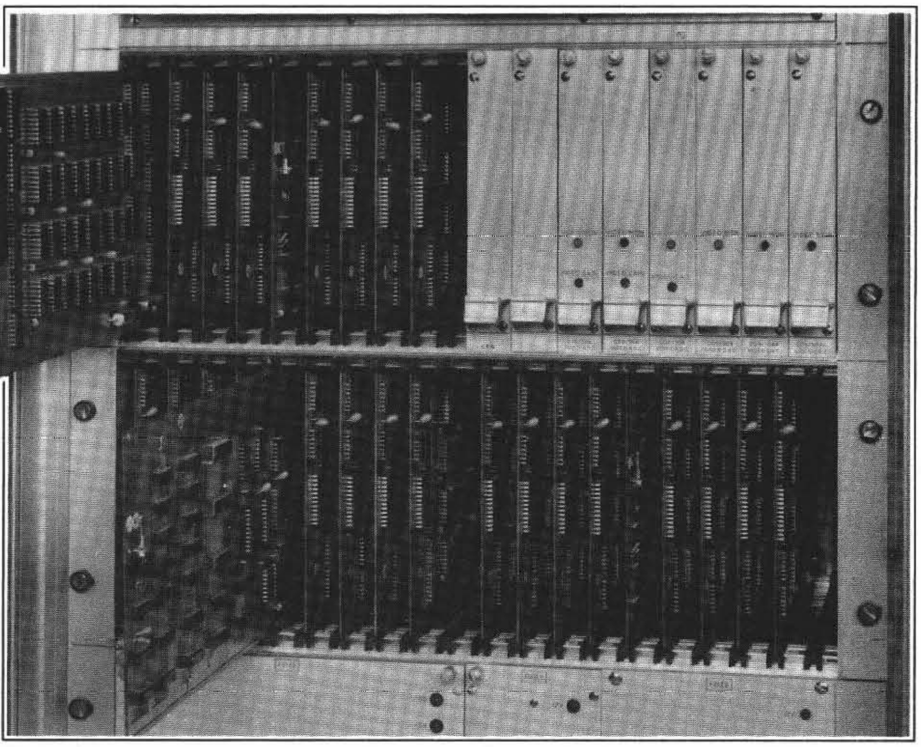

Fig. 8 - A general view of the RGB picture store together with the analogue-to-digital and digital-to-analogue converters.

for minimising circuit complexity. This also meant that the picture storage could be divided into two independently accessible field store sections as shown in the block diagram of Fig. 9 and addressed by separate $\overline{\text{CAS}}$ control signals. When a computer access takes place one section of 16 devices is activated and one of these is singled out by the lower significant four bits of the computer address.

3.2.3 Store control

Each store cycle of 16 video sampling clock periods is divided into two independent store accesses which are allocated alternately to video and computer

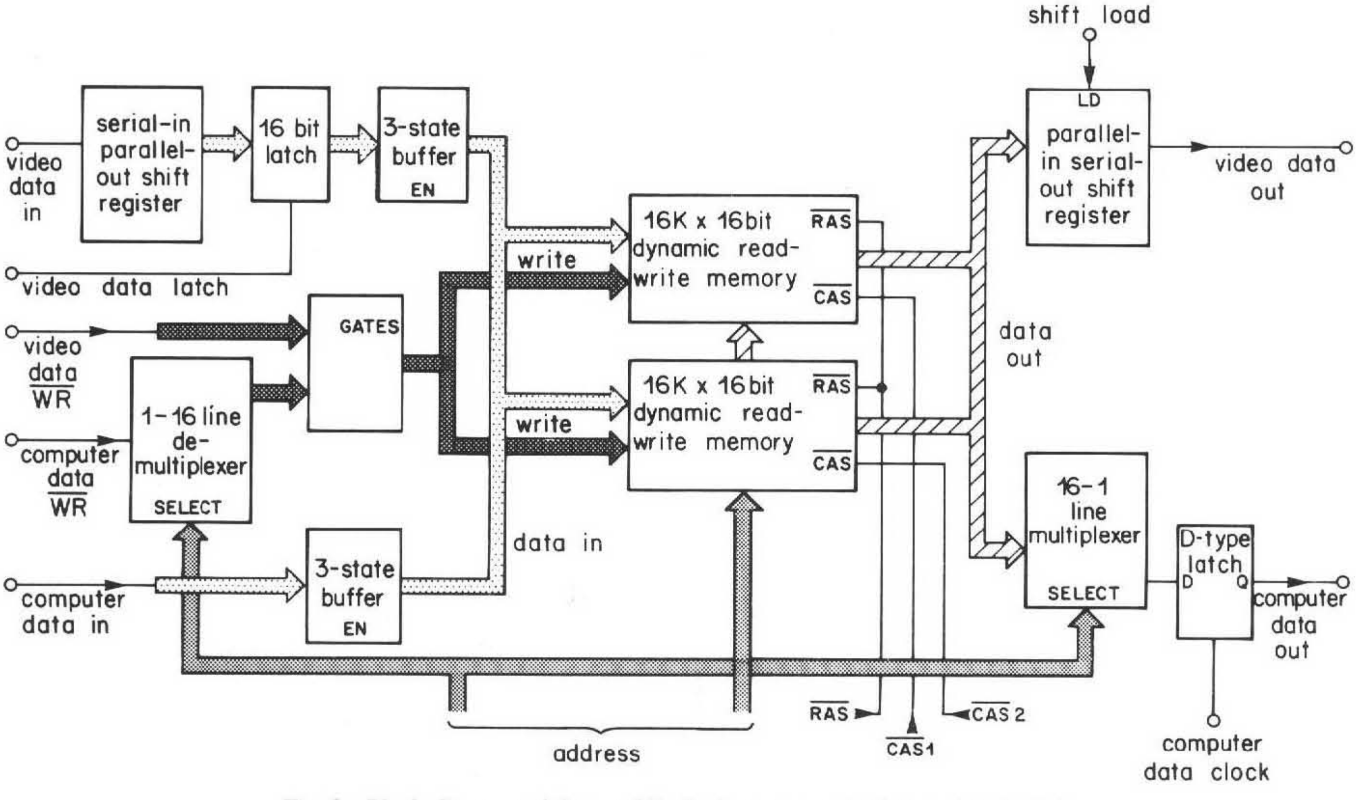

Fig. 9 - Block diagram of the one-bit, single component, picture store board.

use. The video access is normally used for monitoring the contents of the picture store at video rate and at the same time fulfilling a refresh function. The video addresses are generated in counters clocked at the video data sampling rate and locked to supplied mixed synchronising pulses. Addresses are supplied for the active field period only so that the store is blanked in the vertical interval. When required, the video access can be used for writing data to the store at video rate and in this case the reading of video data is interrupted for one picture period.

During a computer data access, the address supplied by the computer command must be synchronised to the store cycle. To accomplish this, the data to be written from the computer memory into the picture store is effectively delayed until it can be handled in the next available store access slot. Data to be read from the picture store is held ready on the store output latches until the computer issues a read instruction to take it.

3.3 Animation store buffers

3.3.1 Introduction

In 1979 a digital television Animation Store system was conceived to provide a mass store for still pictures and a sophisticated range of picture processing facilities[7, 8]. The design was based on an Ampex magnetic disc drive as the main storage element with sophisticated head control and multiplexing to achieve video data rates and real-time data sequence replay. The total capacity achieved was equivalent to 815 pictures and access was controlled by means of a local dedicated computer. Besides the storage and retrieval of stills, several other features were implemented. These included the ability to 'grab' pictures and sequences into the store at video rate and an interface to a video rostrum camera system whereby stills and sequences could be generated manually and animated sequences could be assembled. Chromakey facilities were provided to allow the electronic mixing of pictures to create others.

At an early stage in the development it was decided that the digital video signal would be stored in its component form (rather than as a digitised composite signal) in an attempt to produce a better overall picture quality. Had the signal been stored in its composite form, signal processing would have been required to regenerate the PAL eight-field sequence from one or two stored fields. Moreover, where pictures are derived from a local television camera or other sources available in component form, the processes of PAL decoding and encoding could be avoided.

To support the PAL decoding function and to provide temporary buffer storage and display storage facilities, a number of semiconductor memory stores were required. The proposed EBU video component coding standard, at that time, was a system based on 12/4/4 being the sampling frequencies (expressed in MHz) for the luminance (Y) and chrominance components (U and V) respectively. This work was carried out prior to the International Standard[6] for digital video which subsequently set the luminance sampling frequency at 13.5 MHz and each chrominance component at 6.75 MHz. The buffer stores are required to operate asynchronously so that data may be moved into or out of them without relation to the phase of the signals maintaining the store cycle. The storage is addressed by line labels in the same manner as that described in Section 3.1.1 and one control function of the computer is to keep track of the line numbers allocated during writing and reading operations.

A block diagram of the store arrangement is shown in Fig. 10: the video data paths are near the top and the control functions below. The digital video components are multiplexed to be alternately Y and UV and in this case are allocated eight bits per sample. The main storage boards are arranged to hold one bit each of one picture of YUV — a total of 655 Kbit. Separate video input and output buffers provide the opportunity to synchronise the writing and reading sampling phase to the store cycle and adjust the data delay in single sampling period steps to overcome the finite minimum block size demanded by the store multiplex. Independent Y and UV output processing blocks allow simple operations to be performed on the video data prior to being read out: examples are picture inversion, linear movement in the horizontal or vertical directions or a mixture of each and also the addition of video blanking. The video data is transferred to and from the store using ECL logic levels because of the greater ruggedness it gives to signals over the long video data paths involved between racks of equipment. The function of the computer in this design is purely to control the store: there is no transfer of computer data possible into the main storage blocks.

3.3.2 Store board organisation

The semiconductor bit-plane board is based on 16 K x 1 DRAMs with a 375 ns random read-write cycle time. At a 12 MHz sampling frequency there are about 370,000 data samples generated in a picture period and the storage of these requires a minimum of 22 devices. To give some margin and to allow the storage to be divided four ways in a similar manner to the $4f_{sc}$ store described in Section 3.1 a total of 24 devices are allocated to the main Y store. This means that there are six devices per block and a video demultiplex factor of six is acceptable to match the devices to video rate. The *U* and *V* chrominance components can be supported in eight devices each and are time-multiplexed in a block of 16.

The store multiplex is kept at six and the time-multiplexed phasing of the luminance and chrominance components is shown in Fig. 11. A block diagram of the store board is given in Fig. 12 and shows the video multiplexing and demultiplexing functions resident on-board.

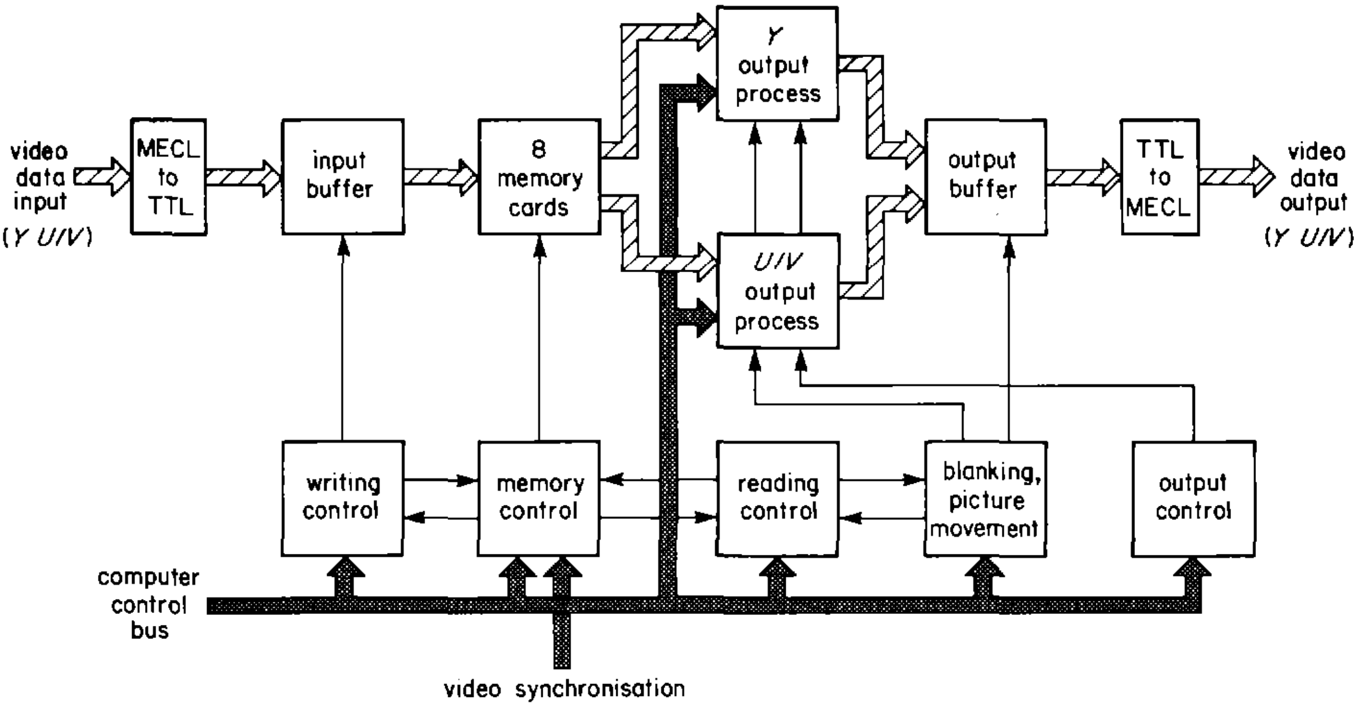

Fig. 10 - Block diagram of a YUV picture store with post-storage processing facilities.

3.3.3 Store control

Apart from the main store board control signals, such as $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, write enable and memory addresses, which are similar to stores already described, this store design differs in its post-processing facilities and only these are referred to here. Their control is handled in the 'blanking and picture movement block' shown in Fig. 10 and allows pictures to be re-positioned on replay.

The computer supplies *X* and *Y* offsets to define the amount of movement required horizontally and vertically. To accommodate a total shift range of one picture width and one picture height the normal propagation delay of the video data through the *Y* and *UV* output processing blocks is made equal to one line and one picture period. The horizontal shift value is added to or subtracted from a value which is loaded into a horizontal counter incremented at the video sampling rate so as to produce a suitably delayed 'start of line' pulse and appropriately phased start and end trigger to generate video blanking. The vertical shift value is used to appropriately delay the time at which the first stored line is read out and when reading ends. From both the horizontal and vertical offset information a mixed video blanking signal can be generated and also a 'background' control which is responsible for filling in the part of the display area from which the picture has moved, with either blanking level or some other colour specified by the computer (possibly intended for chromakey application). In addition to this 'dynamic' picture movement there is a further 'static' offset facility which allows re-timing of pictures within the Animation Store as the internal configuration changes in normal use.

4. THE 64 K GENERATION

4.1 A general purpose digital storage card

4.1.1 Introduction

During 1981 a versatile-digital storage system was developed based on 64 K x 1 bit dynamic memory devices.* Previous general purpose store designs had tended to be over-complex in an attempt to accommodate all possible users. The new system design philosophy aimed to limit circuit complexity by making it dependent upon the user's system requirement. Fig. 13 shows a typical organisation of the component parts: it includes one computer port, four video ports (which may be input or output), a refresh

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* N.E. Tanton was largely responsible for this work.

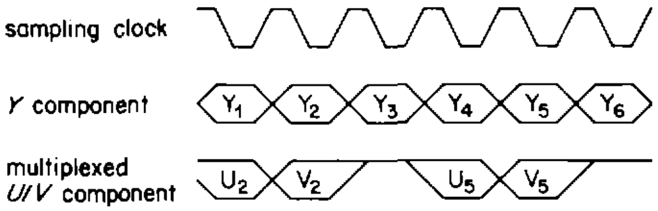

Fig. 11 - The Y and multiplexed UV digital sampling arrangements for the YUV picture store.

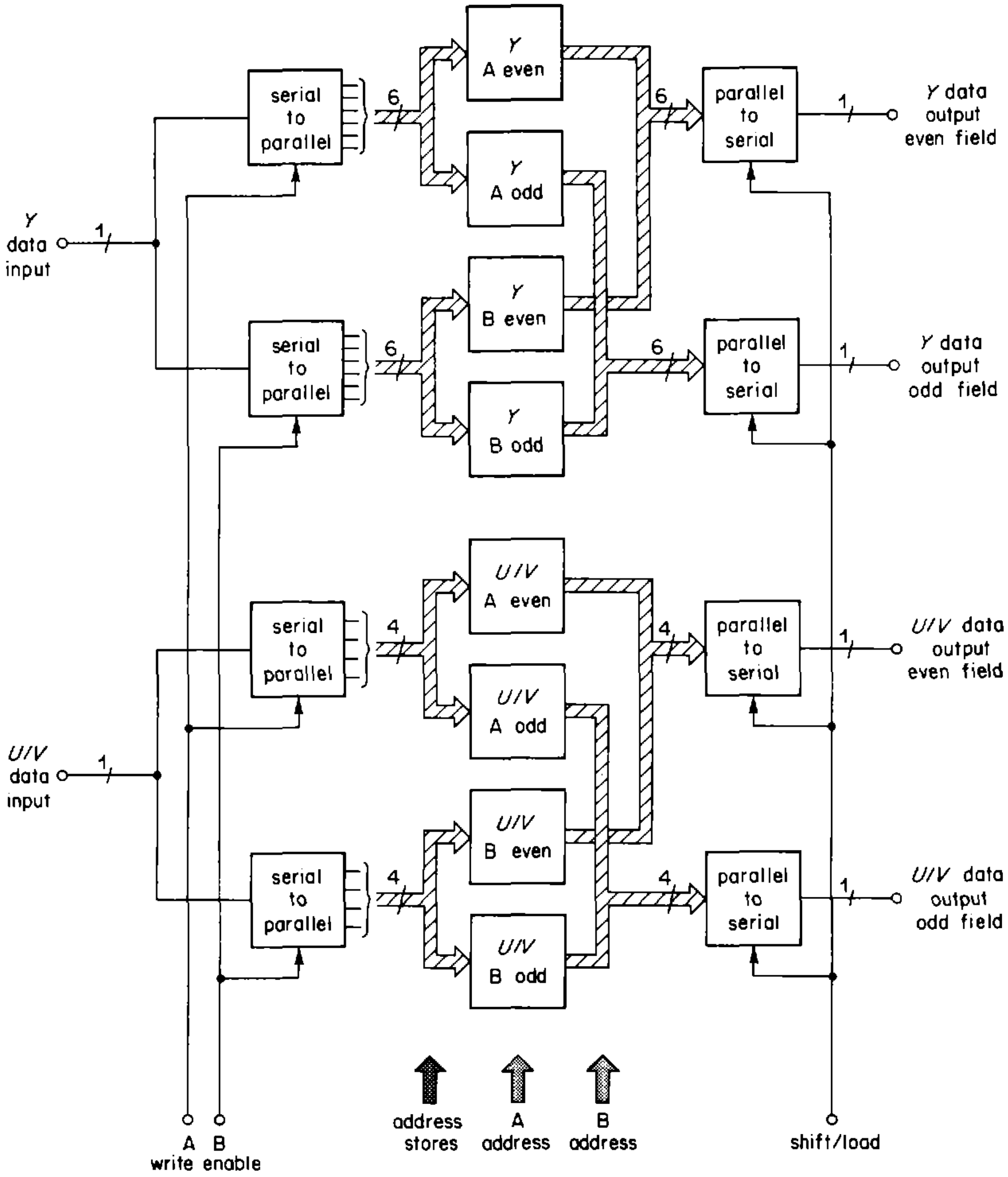

Fig. 12 - Block diagram of a one-bit YUV picture store board.

port to supplement the default refresh provision (if necessary) and a priority arbiter to oversee the system management.

As a compromise between complexity and versatility it was proposed that the new store should consist of a common set of identical storage cards together with a set of user-specified access ports. Communication between the modules would be via parallel address, data and control buses, all under the control of the priority arbiter. The external system behaviour is determined by the access ports and priority scheme, which is specified by the user to suit his application. For instance, a simple picture delay with identical input and output data rates requires one write and one read access port with an elementary priority scheme. A more complicated application with, say, three read operations at one data rate, a write operation at a second (higher) data rate and a microprocessor random access facility would need three read access ports, a microprocessor access port and a write access port with additional buffering, together with a more complicated priority scheme. The system complexity is directly related to the application, with no unnecessary overheads.

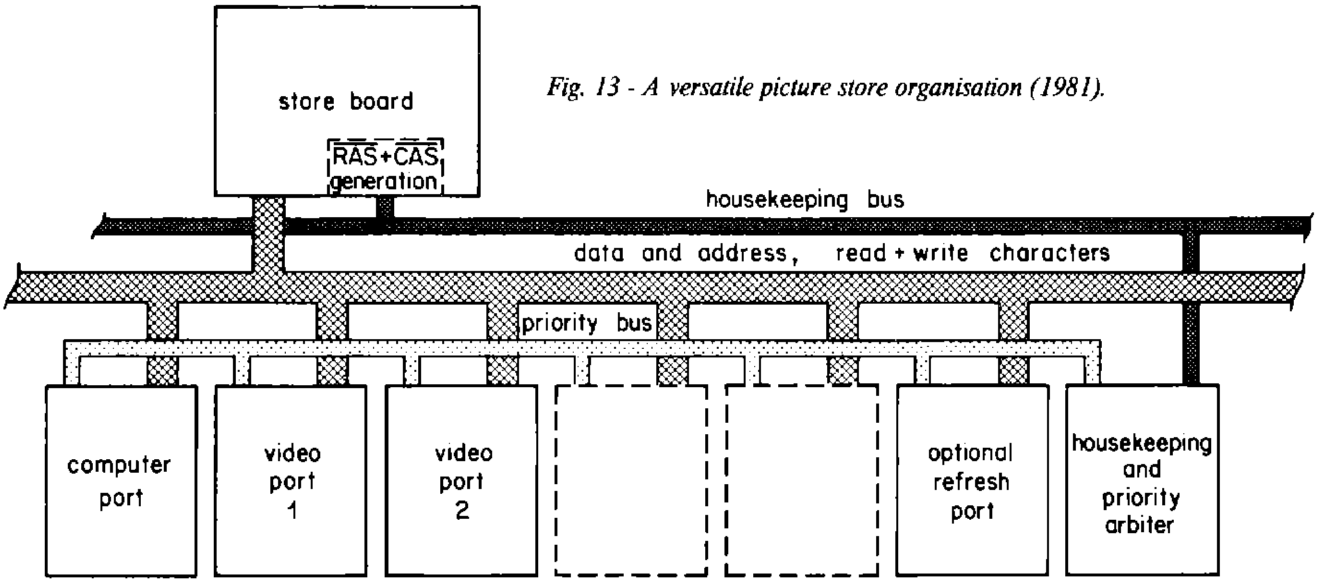
store board
$\overline{\text{RAS}}+\overline{\text{CAS}}$ generation
housekeeping bus
data and address, read + write characters
priority bus
computer port
video port 1
video port 2
optional refresh port
housekeeping and priority arbiter

Fig. 13 - A versatile picture store organisation (1981).

4.1.2 Store board organisation

The store board is built on an 8U BMM card and contains sixty-four 64 K x 1 devices, as shown in the block diagram of Fig. 14. Data is presented to the data bus as a 64 parallel word (1 bit per device) allowing the memory to be configured to suit the user's requirements. The data capacity of a single card is 524,288 bytes which for System I, when sampled at 13.5 Mbyte/s corresponds to just over a complete picture or, alternatively, 2½ fields if only the active line is stored. Each storage location is identified by a 16-bit address A_0 - A_{15}. The remaining four address bits A_{16} -A_{19} serve to select one of sixteen cards. The store card has an automatic refresh facility which operates whenever an idle store cycle occurs. When a refresh cycle is initiated an internal counter is incremented so that each of the 256 pages of dynamic memory is eventually refreshed. The memory devices can be programmed to operate in a normal read or write cycle mode or alternatively in a page mode to shorten the cycle. The maximum data rate of the store can therefore be increased if it is possible to pre-configure the addresses to allow page mode access. The storage card is intended to operate asynchronously at a clock rate which is either chosen to maximise data throughput, in which case an appropriate mix of normal and page mode access cycles is devised, or it is chosen to minimise interface complexity by synchronising the store to the external system clock. A convenient frequency for the first case is 22.22 MHz allowing a page mode access in four clock periods and a normal access in six.

Timings of data, address and control signals on their respective buses are relatively flexible as shown in Fig. 15. The passage of information along the various buses is determined by three signals — input enable (IEN), data enable (DEN) and output enable (OEN). Address, write select and store address signals are accepted by the store on the store clock pulse following the signal IEN, preparing the store fully for its next access cycle. Data is accepted into the store following the signal DEN, and is stored in the address specified under IEN, provided that a write access was specified and the store selected. In the event of a read access, output data becomes available some time after IEN and generally after the IEN of the following cycle. Output data is allowed onto the data bus by the signal OEN, which should be timed with respect to its *own* IEN.

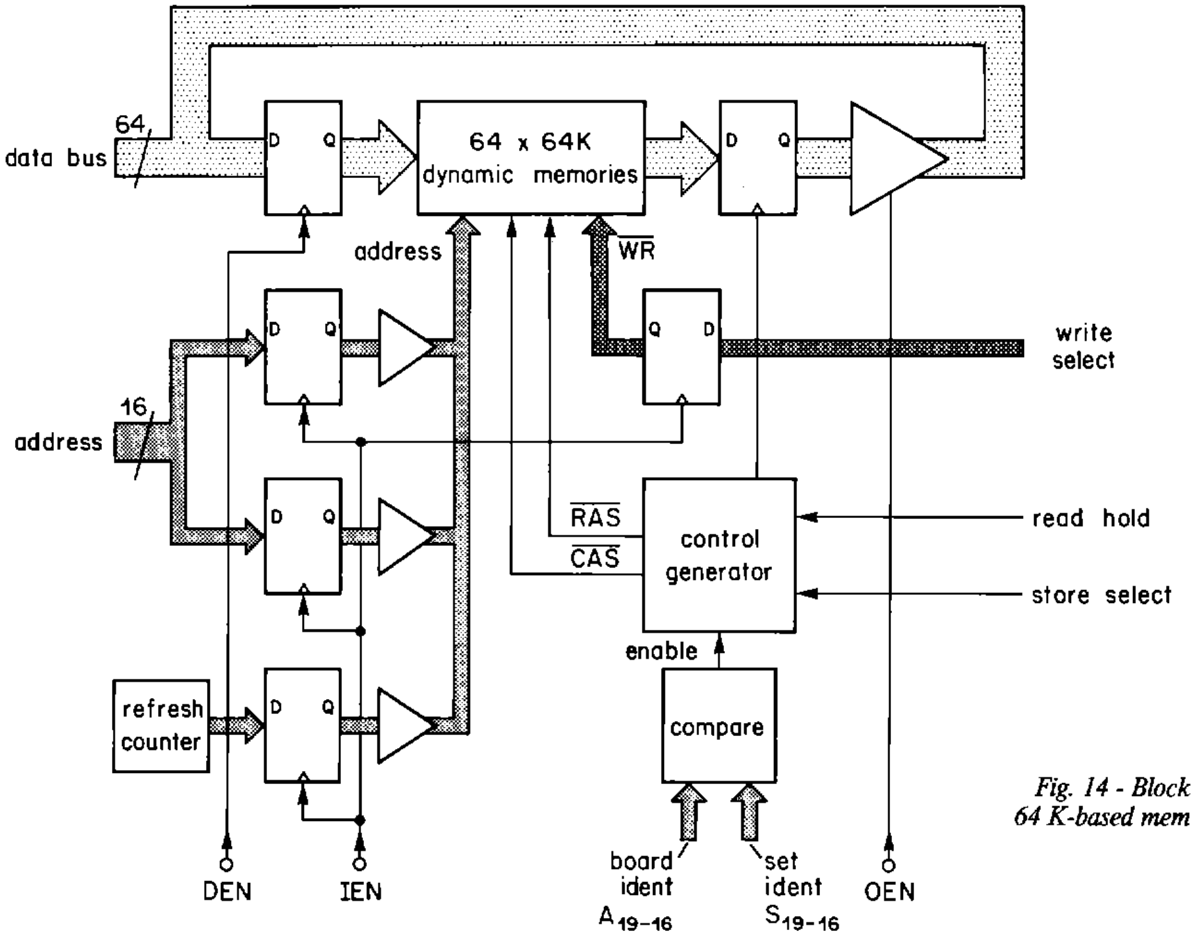

Fig. 14 - Block diagram of a 64 K-based memory store board.

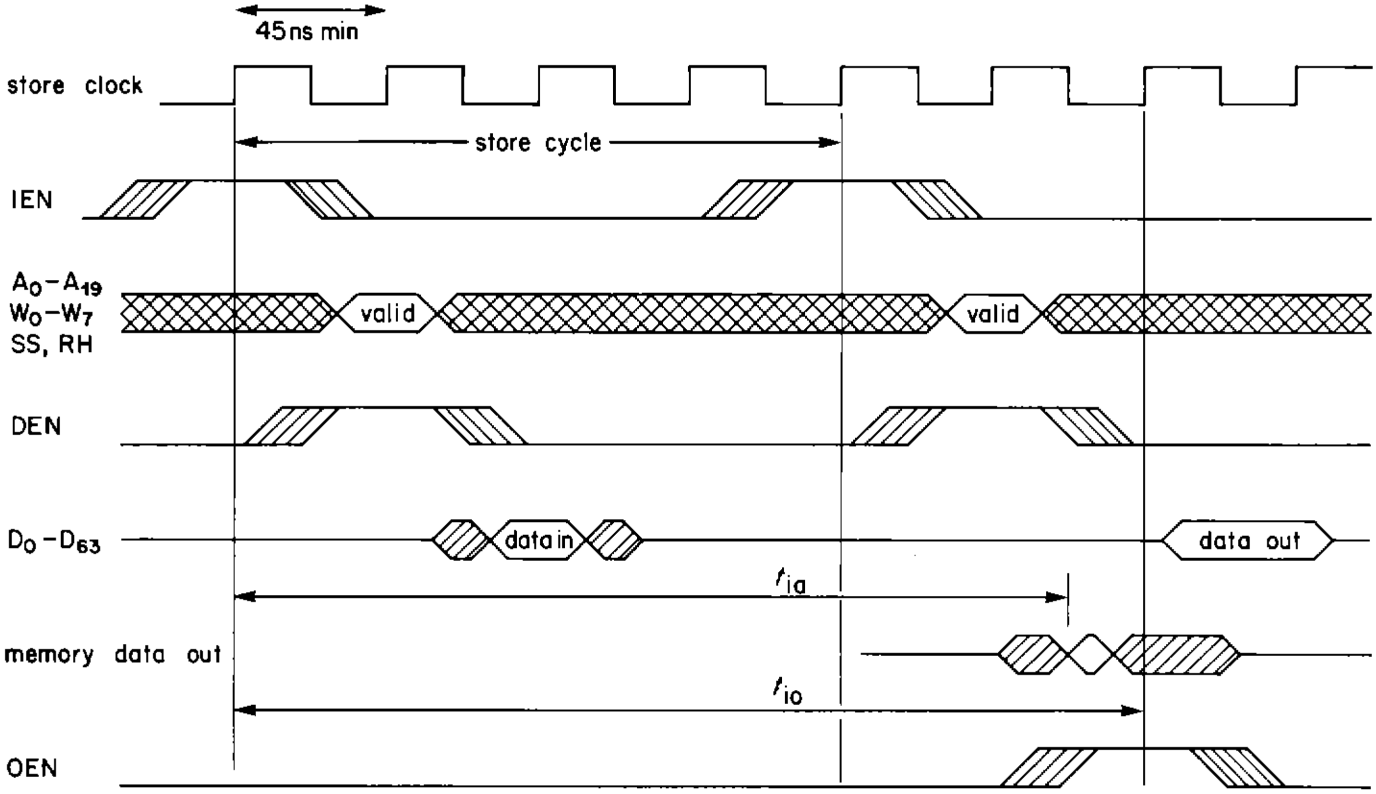

Fig. 15 - Memory store board control signal requirements.

4.1.3 Film dirt concealment application

This application requires a storage system capable of providing four simultaneous digital video outputs while accepting one digital video input, all at 13.5 Mbit/s[9]. The four outputs correspond to points in four consecutive fields scanning in unison: outputs 2 and 3 are the even and odd fields of a picture and fields 1 and 4 are the nearest odd and even fields respectively from the two adjacent pictures.

The first decision is to establish what data demultiplex factor is needed to allow five consecutive store accesses per store cycle. An 8-way demultiplex has a store cycle length of 592 ns, which is sufficient only to allow two normal or three page mode accesses at the full store speed of 22.22 MHz. A 16-way demultiplex has a store cycle length of 1184 ns which is long enough for 4N, 2N + 3P, or 6P accesses at full speed where N = Normal and P = Page. Also with a synchronous store clock of 13.5 MHz it is possible to accommodate 4N or 1N + 4P accesses. Of these possibilities, 2N + 3P and 1N + 4P look most promising. The 1N + 4P scheme is attractive because it uses a 13.5 MHz clock and can be made synchronous. Unfortunately, it is difficult to implement because the requirement for an adjustable propagation delay implies a non-static address sequence and it is not always possible to guarantee that four out of five accesses can be made with the same memory row address. The 2N + 3P option, despite its attendant problems of asynchronous operation, is, therefore, chosen.

This system has been tested using a computer model to investigate the maximum buffer sizes and worst case access sequences imposed by the rest of the equipment. The main parameters of the model are store access time, write block length and read block length (sixteen times the write and read clock periods respectively) and whether the addresses are singly or doubly buffered. Two additional parameters called 'write address down time' and 'read address down time' are included to imitate the time taken for addresses to change.

Assuming that the four read ports are singly buffered, the results of the simulation indicated the level of buffering required for the write port, for a given input data rate, and whether additional refresh arrangements were required.

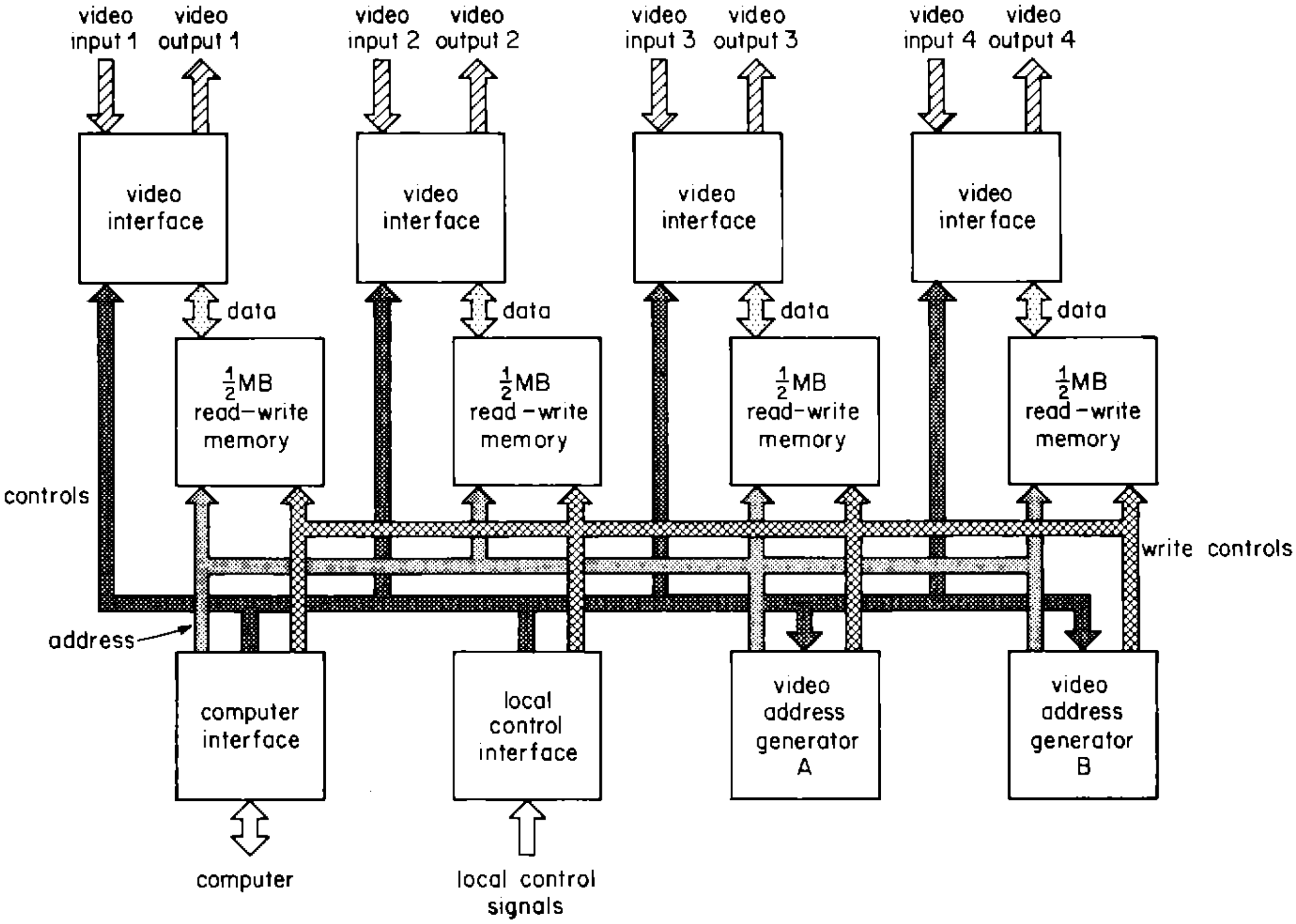

Fig. 16 - 2 Mbyte picture storage module based on 8U store boards.

The application can be satisfied with five, albeit more complex, ports and two store cards giving a store efficiency of 98.7%, and refresh requirements are handled entirely by the default mechanism resident on the store boards.

4.1.4 A 2 Mbyte storage module

For a random access application the basic architecture of Fig. 13 was modified so that the total video input and output data rate could be increased, particularly with high definition television (HDTV) applications in mind. Four of the general purpose store cards were interconnected via a common address and control bus, as shown in Fig. 16, but the four video access ports are provided on video interface boards with independent local data bus connections to each store card. Other control functions which are handled on separate cards include the generation of video addresses, control interface and computer interface. The total storage amounts to 2 Mbyte, with a potential maximum video data rate corresponding to a bandwidth of more than 54 MHz.

The storage boards are operated on a synchronous (13.5 MHz) eight-way video demultiplex cycle whose timing diagram, presented in Fig. 17, is based on the general waveforms of Fig. 15. The eight clock-period store cycle is split into two independent access slots, referred to as A and B. The A slot is used exclusively for video reading to provide a monitor display of the store contents and fulfil refresh requirements (independently of the default refresh function incorporated within the store boards). The B slot is used either for a second video access or a computer access allowing both writing or reading. When the second video access is used for writing, the video input is stripped of its line codes and the synchronising information is used to lock the scanning control for slot B accesses. Video addresses, which are independently generated for the A and B access slots, can be modified, partly by firmware and partly by software, to alter the scanning ranges of the addressable *X, Y, Z* coordinates which specify the horizontal (picture width) dimension, vertical (picture height) dimension and the depth (frame number) dimension respectively.

The computer interface (DR11W) is based on a 16-bit data bus together with control signals for RECEIVE, SEND and DATA FUNCTION CONTROL. There are eight types of data function provided and these include computer data input or output, loading an *X* or *Y* coordinate address, post-auto incrementing those addresses by one, two or four units and store module number. The remote coupling of the store to the computer, in this way, means that it is difficult to use the storage as 'working memory' because of the penalty in access time. Thus, in normal operation, a data area from the store is read into the computer for processing to be performed before transferring it back again for direct viewing in real time.

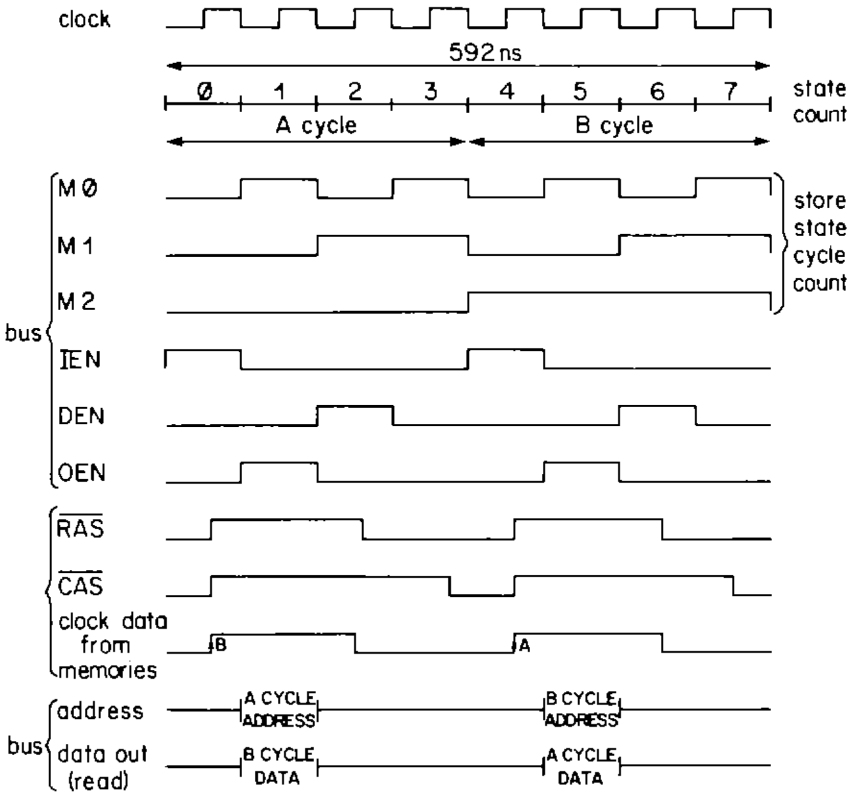

Fig. 17 - The 2 Mbyte picture store control signal waveforms.

4.1.5 High definition television application

The potentially high data rate of the 2 Mbyte storage module makes it suitable for an HDTV display store. Three modules have been used to hold three components of a video signal, *R*, *G*, and *B* as shown in Fig. 18. The four video output signals from each 2 Mbyte module are fed into a multiplexing unit which combine them into a 54 MHz serial data stream before being passed on to high-frequency d.a.cs.

The 54 MHz clock is generated locally and drives a multiplex unit associated with each module. Counters generate the video synchronising information to control each module and provide a mixed synchronisation signal to accompany the video output.

Independent computer access, at a slow rate, is available via the DR11W computer interface and it would be possible with suitable demultiplexing units, to provide for an HDTV real-time signal input, at a future date.

4.1.6 Sequence store application

To fulfil an immediate requirement to provide a basic, albeit small, storage capability for short video sequences, three of the 2 Mbyte modules have been arranged with sequencer units shown in Fig. 19. The sequencer units allow the video signals, sampled at 13.5 MHz in this case, to be directed to and from the individual store boards according to the sequence control which supplies the necessary video synchronisation and board decoding signals.

The control of the sequence store is sufficiently flexible to allow the following configurations:

a) Video data coding can be *RGB*, *YUV*, *Y* or PAL, etc., at 8 bits for each component.

b) The architecture can be effectively changed to accommodate four *RGB* stores, one HDTV store, six *YUV* stores or twelve *Y* only stores.

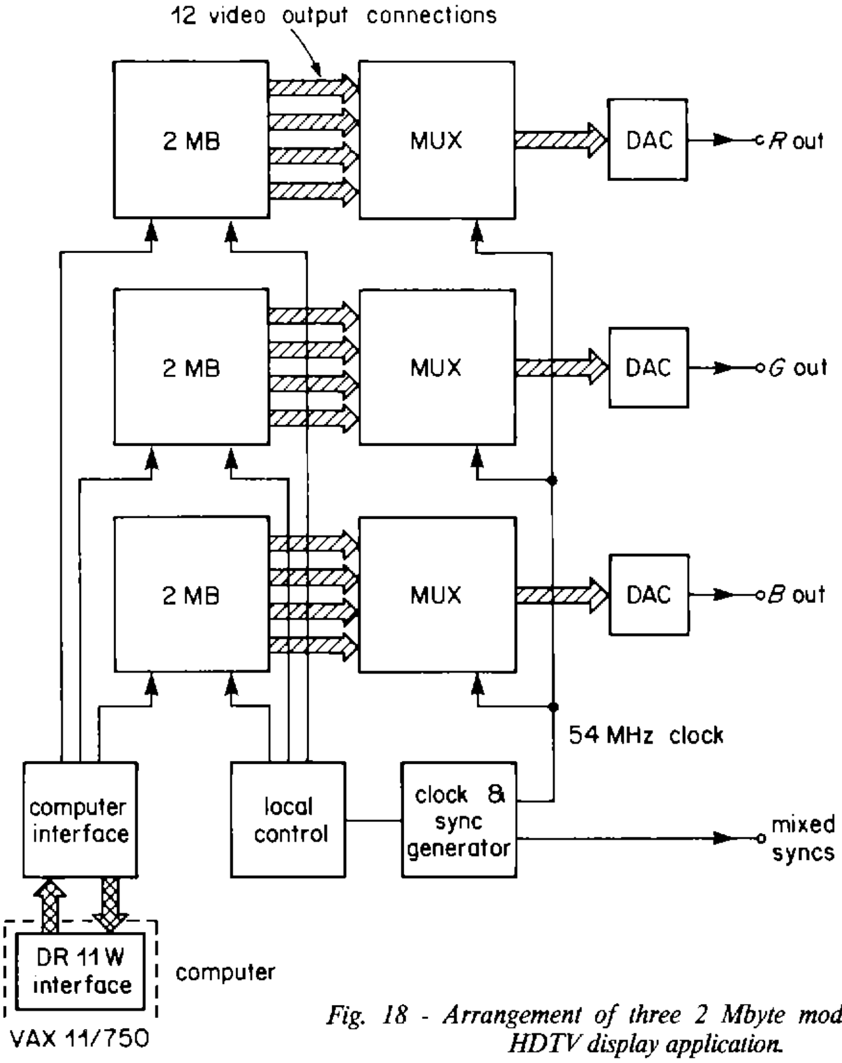

Fig. 18 - Arrangement of three 2 Mbyte modules for an HDTV display application.

c) Partial picture sizes can be used to increase the sequence length at the expense of picture area. Fixed fractions of one-half and one-quarter are provided.

This allows a number of optional sequence arrangements which include, for a 625-line System I standard:

i) 12 *Y* pictures (about 0.5 second)

ii) 24 *Y* pictures, half-area (about 1 second)

iii) 48 *Y* pictures, quarter-area (about 2 seconds)

iv) 24 *YUV* pictures, quarter-area (about 1 second)

The sequences can either be repeated cyclically, causing a 'hiccup' to occur in between sequence transitions, or palindromically so that a continuous display can be formed. Although it is bulky in terms of hardware and suffers from the limitations of the DR11W interface this equipment has provided a beginning for the image processing of short sequences. A general view of the equipment comprising the short sequence store is given in Fig. 20.

4.2 A compact random-access picture store

4.2.1 Introduction

A television semiconductor picture store of 1.5 Mbyte capacity and capable of holding an *R*, *G*, *B* picture when sampled at 13.5 MHz has been described[5] as part of equipment built to study enhanced teletext. In addition to the ability to read or write pictures at the full video rate, it is possible to read or write data at a slower rate under the control of a local microcomputer. So popular had the teletext equipment become that it became necessary to consider duplicating it. The pace of technology, however, over the three

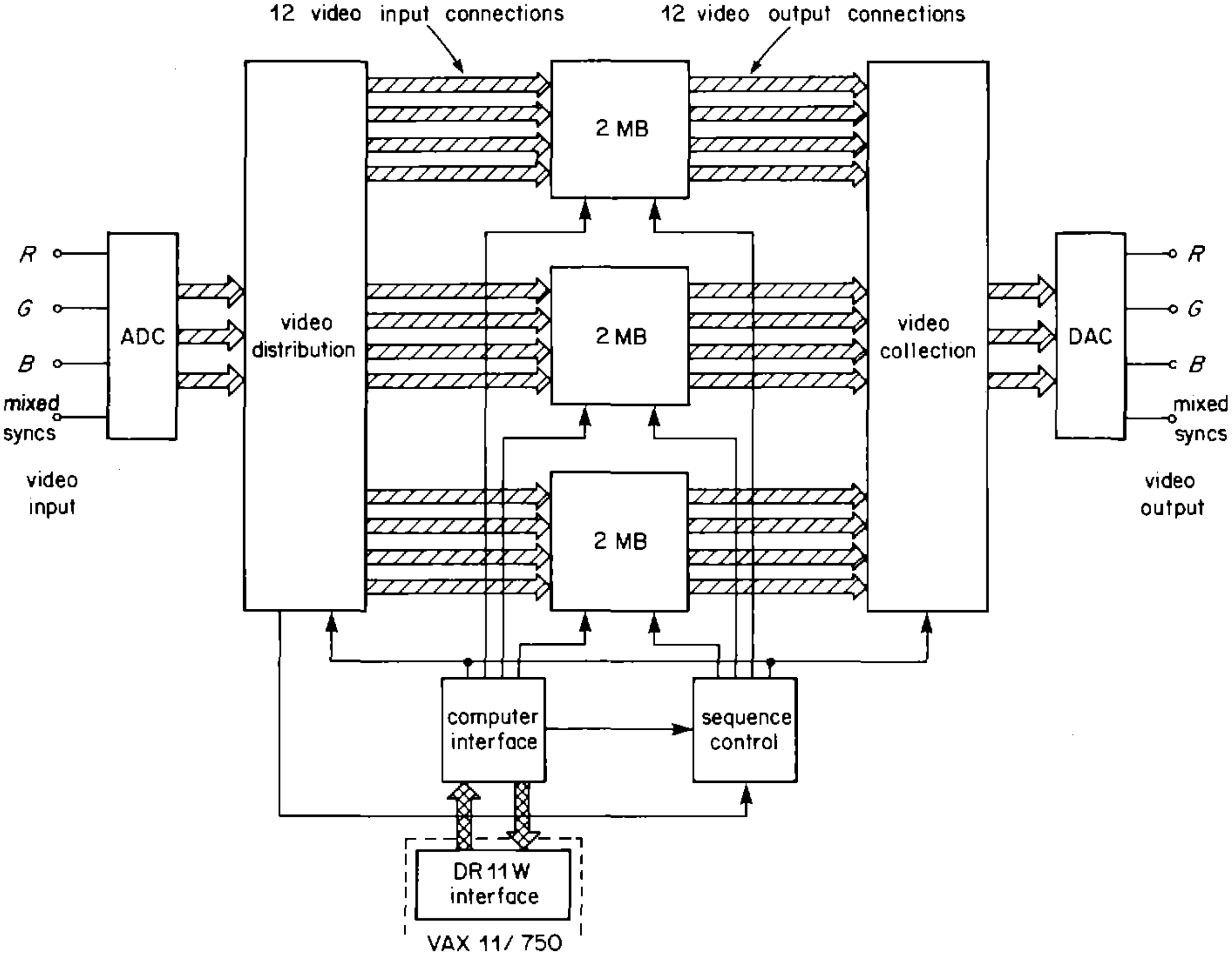

Fig. 19 - Arrangement of three 2 Mbyte modules for a short television sequence store.

years since the original design, made it worth considering a re-design of the semiconductor store using the latest available generation of dynamic memories — namely 64 K devices (256 K dynamic memories were becoming available but at prices which would not become cost-effective until 1985). A new design held out the promise to be more compact, cheaper to build, cheaper to operate because of lower power consumption and lower heat dissipation — and also, to operate with an improved performance margin.

The original store design contained one 4U p.c.b. for each bit of each *R*, *G* and *B* component — making 24 memory boards in all — see Fig. 8. Each *R*, *G* and *B* component required one 4U control p.c.b. and a further three interface boards to connect the store to the microcomputer, housed in a separate rack. The power supplies (+5 V, +12 V and −5 V) were contained in an additional rack making a total of 30 p.c.b.'s plus power supplies spread over four standard equipment racks.

A new design made it possible to reduce the number of 4U memory boards from twenty-four to six. By combining a number of the store control functions of the *R*, *G* and *B* stores, the three original control boards could be replaced by one. Also, the considerably fewer number of store boards could be connected directly to the computer bus itself, thus dispensing with the three interface boards. The whole *R*, *G*, *B* store, could therefore be built on seven boards occupying just over a quarter of one 4U rack. The 24-bit picture store, shown as a block diagram in Fig. 21, dissipates less than 50 W.

4.2.2 Store board organisation

Using memories with 64 K address capability a video multiplex factor of eight permits the required dual access port capability with relatively little extra capacity over the minimum required for an active picture when sampled at 13.5 MHz. On this basis a picture store built with 64 K dynamic memories requires just eight chips per bit. It is possible, in

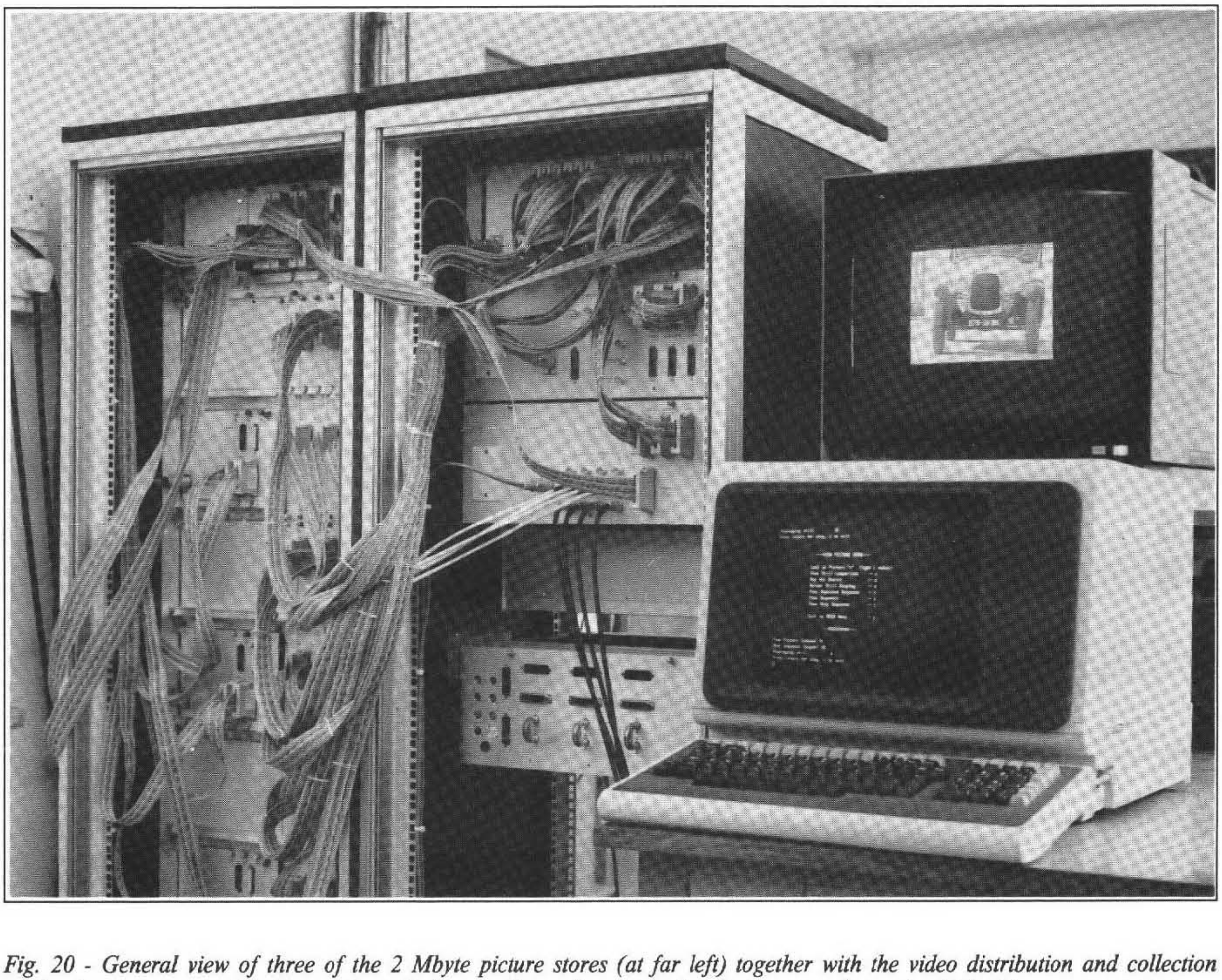

Fig. 20 - General view of three of the 2 Mbyte picture stores (at far left) together with the video distribution and collection hardware, computer interface, picture display monitor and computer terminal arranged as a short television sequence store.

practice, to accommodate about 30-40 memory chips in 16-pin or 18-pin DIL packages together with multiplexing and demultiplexing chips on a 4U p.c.b. This suggests that four bits per board is a reasonable aim for a convenient storage unit. There is little to choose between the 64 K x 1 or 16 K x 4 options as either is suitable, but the latter was chosen (type IMS 2620-12) and the p.c.b. layout was simplified because of its common data input-output connection.

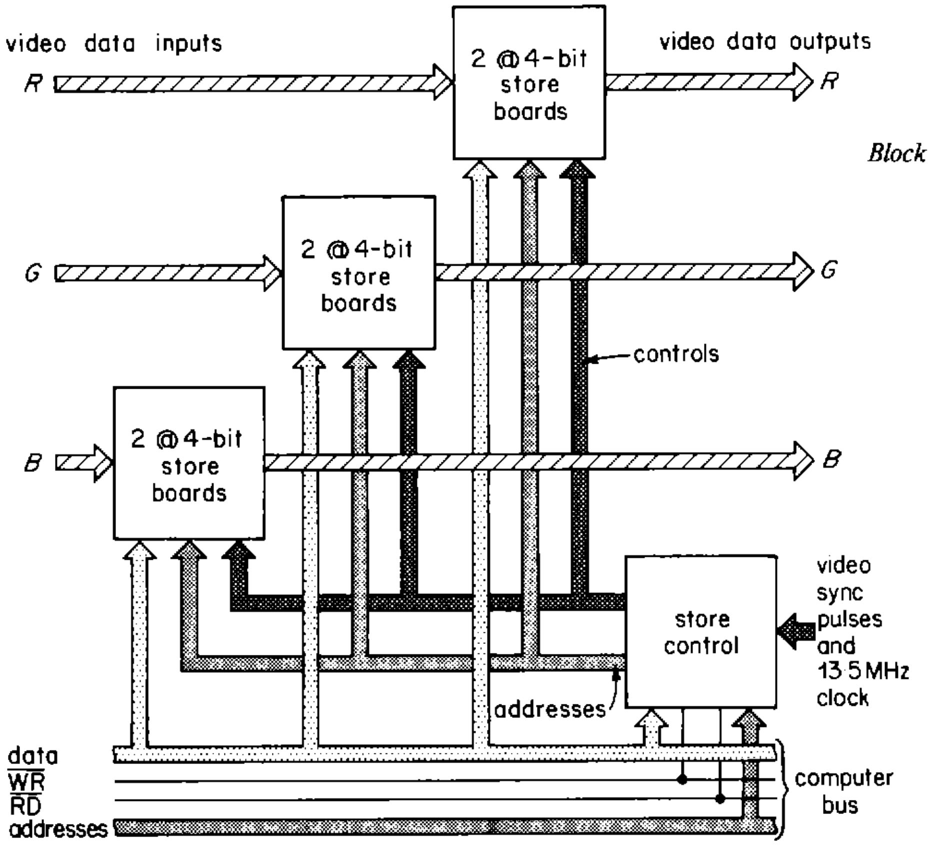

Fig. 21
Block diagram of compact RGB picture store.

A block diagram of the memory board is shown in Fig. 22. The thirty-two memory chips are arranged in four groups of eight. They all receive a common address input but each group is fed with a different version of $\overline{RAS}$ and $\overline{CAS}$ which in effect act as a further two address bits to identify one group out of the four. Data can be written to and read from the board in two ways each. Video input data is clocked into a serial - parallel shift register and every eight clock-periods eight data samples are stored in one of the four groups of memories. Similarly, video output data is formed by reading out data from one of the four groups of memories and supplying it to the eight inputs of a parallel - serial shift register. Data can also be transferred into and out of the board at a slower rate of 13.5 ÷ 8 Mbyte/s by means of the computer bus. The computer address associated with a computer command is converted into a store board address on a separate control board and supplied to the store board along with the other control signals, including a 3-bit address referred to as $X_2 - X_0$ which selects one of eight memory devices in the multiplex block.

4.2.3 Store control

The control signal waveforms associated with a read and a write cycle for the Inmos 16 K x 4 memory chip IMS 2620-12, as used in the store, are given in Fig. 23. $\overline{CAS}$ is fed into an active delay unit, with stated accuracy of ± 2 ns, before being applied to a pair of fast buffers and the memory chips. The effect of this is to offset the $\overline{CAS}$ waveform from the row-column address transition to meet the column address set-up criterion and ensure that the slower mid-speed option of the memory device can be used. Alternate memory cycles are used exclusively for video reading to continually monitor the contents of the store and provide refresh. The other memory cycle is used for a video write access or a computer data access, either reading or writing.

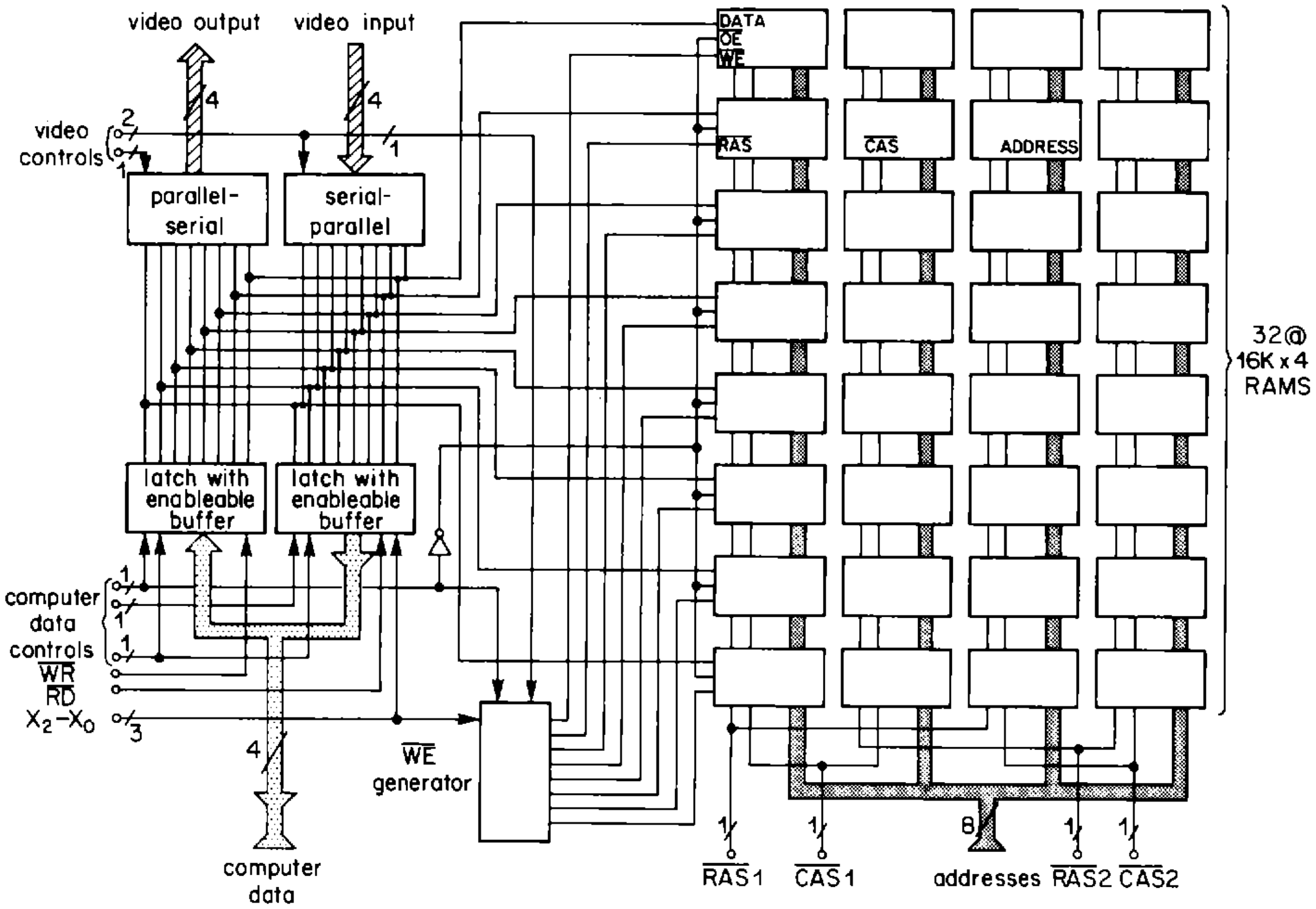

Fig. 22 - Block diagram of the 4-bit store board.

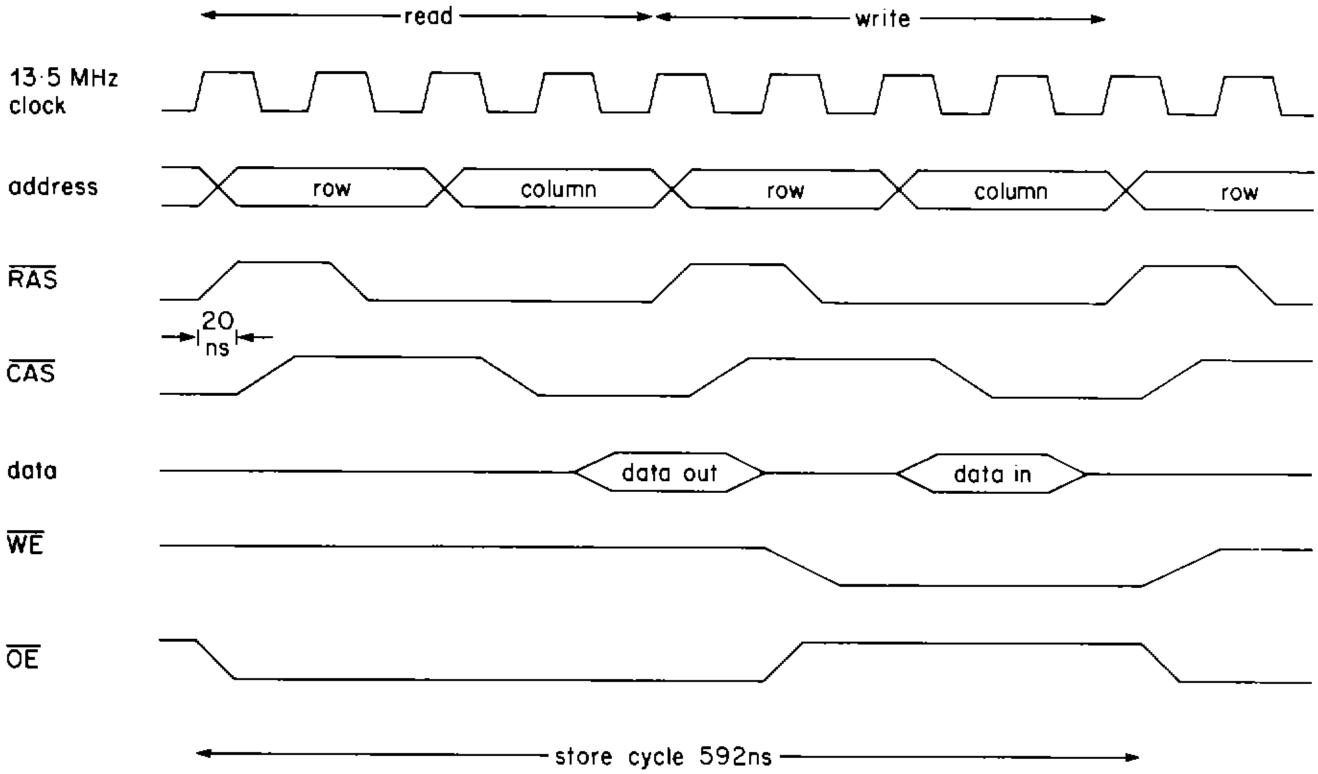

Fig. 23 - Control signal waveforms for a READ and WRITE cycle of a type IMS 2620-12 read-write memory.

The video 'grab' function is provided in addition to and not 'instead of' the video read function although when the store is grabbing a video picture, the computer data transfer process is interrupted. This allows the video input to the store to be monitored continually while the grab operation of a single picture is executed. In addition to a picture grab, a field grab may be requested and also a field repeated in both halves of the store to achieve, crudely, a non-flickering field grab of moving picture material.

Computer access serves three independent blocks of storage containing 524,288 bytes of data addressed on an X-Y coordinate basis where X, $Y = 0$, 0 represents the top left corner of a display of the store contents and X increases horizontally to the right and Y increases in a downwards direction. An auto-increment of X, Y address can be invoked by nominating different computer input/output (I/O) ports in the computer data transfer process. Nine ports identify a static shift and one of eight directional shifts along either axis in either direction or any of the four intermediate diagonal axes. This has proved essential for high-speed data transfer between the store and an external storage device such as a Winchester disc drive.

A full list of the computer commands associated with the store is given in Table 2. The first column indicates the input-output direction of the computer data transfer — input means into the computer memory and output means out of the computer memory. For example, when a computer input instruction is given to the computer port address 1E0, data is read from the store holding the green video component at the current X, Y pixel address and the X, Y counters are not auto-incremented. As well as video data transfer the instruction list includes commands to instigate the video 'grab' function and load a new X, Y pixel address.

5. DELAY APPLICATIONS

5.1 Short video delay

A 64-bit static memory chip, with an access time of 25 ns (type Am 29701), provides a means of producing short, variable video data delays. To give a comfortable operating margin the devices are demultiplexed two ways and operated in A and B sections[1]. Each device is arranged as 16 x 4 bits so that a minimum of four are needed to service eight bits. Data is read from address n in section A while data is written into address n-1 in B. During the next clock period, data is written into address n in A and read from n in the second. The delay is governed by the length of the address sequence and is quantised into multiples of two sample periods. Delays of odd numbers of periods are achieved by selecting the input or output of an additional D-type latch at the delay output. The range of delay possible with this configuration, shown with its control signal generation chips, is three to thirty-three clock periods. A simplified block diagram of the arrangement is shown in Fig. 24.

5.2 Television line delays

Several versions of television line delay units have been designed and constructed on 4U BMM cards. All require a two-way demultiplex to match video rates and their delay setting control is similar to that described in Section 5.1. The first — see Fig. 25(a) — is a dual line delay organised as two completely independent blocks of up to 1028 8-bit words. The delay for each block can have one of two values, each of which is preset on a switch mounted on the printed circuit card and selected by separate control inputs. The second (Fig. 25(b)) is a quadruple line delay organised as four blocks of up to 1028 8-bit words, each block having separate data inputs and outputs but sharing a common delay setting which is preset by an on-board switch. Both these units are based on Fairchild 256 x 4 bit static read-write memories type 93L422 or 93422, depending upon the required operating speed. These devices have worst case read access times of 60 ns and 45 ns respectively.

The third unit contains four 10-bit delays connected in tandem with a common delay setting as shown in Fig. 25(c) and was designed at a later time when Intel type 2148 HL-3, 1K x 4, static devices became available. The access time for these is 55 ns. Four and two half-devices are required for each delay making a total delay range of between 1 and 2049 clock periods which corresponds to more than two television lines of a digital video signal sampled at 13.5 MHz. The single and dual clock periods of delay are achieved by de-selecting the memory devices and operating them in a power-down fashion.

5.3 Television picture delay

A programmable picture delay board which can be set in the range 20 - 589,852 clock periods delay, has been constructed on a 4U BMM board, using 64 K semiconductor dynamic memory devices and dissipates less than 10 W at 5 V. Each board handles four bits of data. The delay can be directly set by a 20-bit control word or, alternatively, up to 32 delays can be pre-programmed in on-board programmable read-only memory devices and remotely selected by a 5-bit control word.

A primary aim when designing this board was to produce a standard 4U BMM unit which would be

Table 2

I/O Address List for the RGB Store Control

I/O	Port Address	Data	Function
O	1C4	00 Hex	Video write a picture.
O	1C4	01 Hex	Video write a field.
O	1C4	03 Hex	Video write a field and duplicate in both field halves of store.
O	1D0	Xmsbyte	Load *X* msbit's address.
O	1D1	Xlsbyte	Load *X* lsbyte address.
O	1D2	Ymsbyte	Load *Y* msbit's address.
O	1D3	Ylsbyte	Load *Y* lsbyte address.
O	1D8	Data	Shift LEFT and write to all *R*, *G*, *B* stores together.
O	1D9	Data	Shift LEFT and UP and write to all *R*, *G*, *B* stores together.
O	1DA	Data	Shift UP and write to all *R*, *G*, *B* stores together.
O	1DB	Data	Shift RIGHT and UP and write to all *R*, *G*, *B* stores together.
O	1DC	Data	Shift RIGHT and write to all *R*, *G*, *B* stores together.
O	1DD	Data	Shift RIGHT and DOWN and write to all *R*, *G*, *B* stores together.
O	1DE	Data	Shift DOWN and write to all *R*, *G*, *B* stores together.
O	1DF	Data	Shift LEFT and DOWN and write to all *R*, *G*, *B* stores together.
I/O	1E0	Data	Access GREEN store only, no *XY* change.
I/O	1E1	Data	Access RED store only, no *XY* change.
I/O	1E2	Data	Access BLUE store only, no *XY* change.
O	1E3	Data	Leave *XY* alone and write to all *R*, *G*, *B* stores together.
I/O	1E8-1EF	Data	Access GREEN store only but with auto-incremented addresses as detailed in 1D8-1DF.
I/O	1F0-1F7	Data	Access RED store only but with auto-incremented addresses as detailed in 1D8-1DF.
I/O	1F8-1FF	Data	Access BLUE store only but with auto-incremented addresses as detailed in 1D8-1DF.

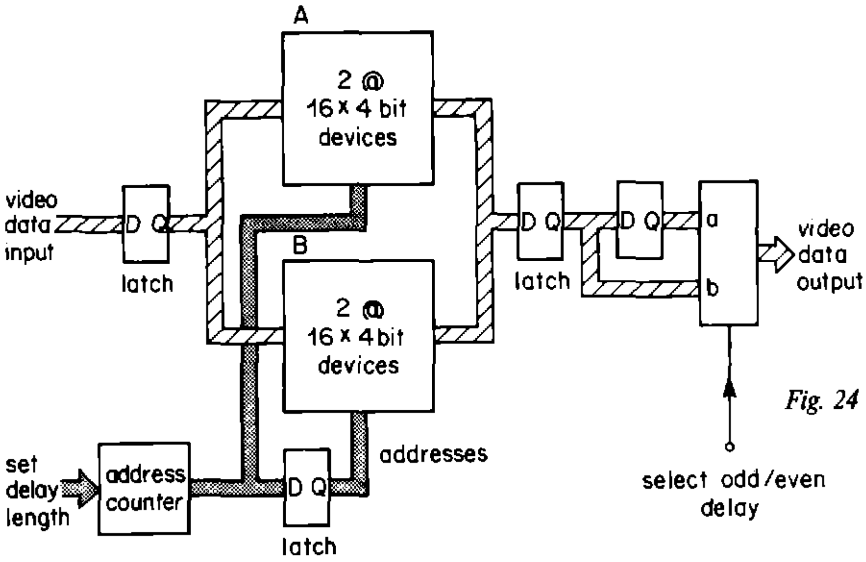

Fig. 24 - Programmable 8-bit short video delay.

self-contained and combine a complete picture store and delay setting control. A further consideration was to make the delay continuously variable and independent of any multiplexing of storage devices. The first solution devised was based on a television field delay with 8-bit wide capacity. There were two reasons why this solution was not adopted. Firstly, the number of chips required to realise the design was far in excess of the number generally accepted to be reasonable for a 4U board. Secondly it was realised that an 8-bit wide unit might cause an unnecessary restriction in data resolution; in many video processing applications nine or ten bit resolution is preferred, if not obligatory. This led to the development of a design based on a television picture with 4-bit wide capacity. The reduced amount of multiplexing due to halving the word-width made a significant difference to the overall chip count which made the design feasible. A real advantage of this arrangement is gained in the board count when more than eight bits of data are handled.

A video demultiplex of nine allows up to 589,824 bits to be stored which is sufficient to hold a full television picture when sampled at 13.5 MHz. A straight 9-way demultiplex has been chosen for three reasons. The minimum memory cycle time of 270 ns requires a demultiplexing factor of at least four which is not a sub-multiple of 9. A nine clock-period cycle allows the devices to be accessed at a rate which is three to four times slower than their design capability. This makes for a lower overall power consumption because the chip dissipation increases proportionally with cycle rate. Also the demultiplexing and re-multiplexing functions for a factor of 9 can be realised with a reasonably economical chip count. The total number of devices required is, therefore, 36 per board. A block diagram of the delay board is shown in Fig. 26.

With this arrangement all devices take the same 16-bit address. The delay is altered by allowing a certain range of addresses only to be generated but instead of the A/B alternate read-write control approach the memories are arranged to operate in a read-modify-write cycle[1]. Data, which was written on the previous access of an address, is read out and subsequently shifted out through the output registers. During the same cycle and at the same address, new current data is written in. Thus the number of addresses generated determines the total delay through the store.

The waveforms associated with one store cycle are shown in Fig. 27. The delay can be continuously altered within the 9-way demultiplex range by changing the relative separation of the clock-edges on which the data is enabled into the input latch using $\overline{\text{G1}}$ and shifted out from the devices using the second data enable signal $\overline{\text{G2}}$ The relative delay, on a scale from one to nine is indicated for each combination of $\overline{\text{G1}}$ and $\overline{\text{G2}}$.

6. THE 256 K GENERATION

6.1 Introduction

Semiconductor dynamic memory chips now offer an alternative solution to Winchester disks operating in parallel for the bulk storage of television pictures required for picture processing by computer. Television picture stores based on semiconductors have proved reliable and repeatable — there are no moving parts to go wrong and once a satisfactory p.c.b. design has been achieved it can be replicated in large quantities. A number of other advantages can be identified. The whole store behaves like a random access memory — each pixel is equally accessible — and there is no need for large separate buffer stores: a very short buffer of less than a micro-second is sufficient to deal with the multiplexing of memory

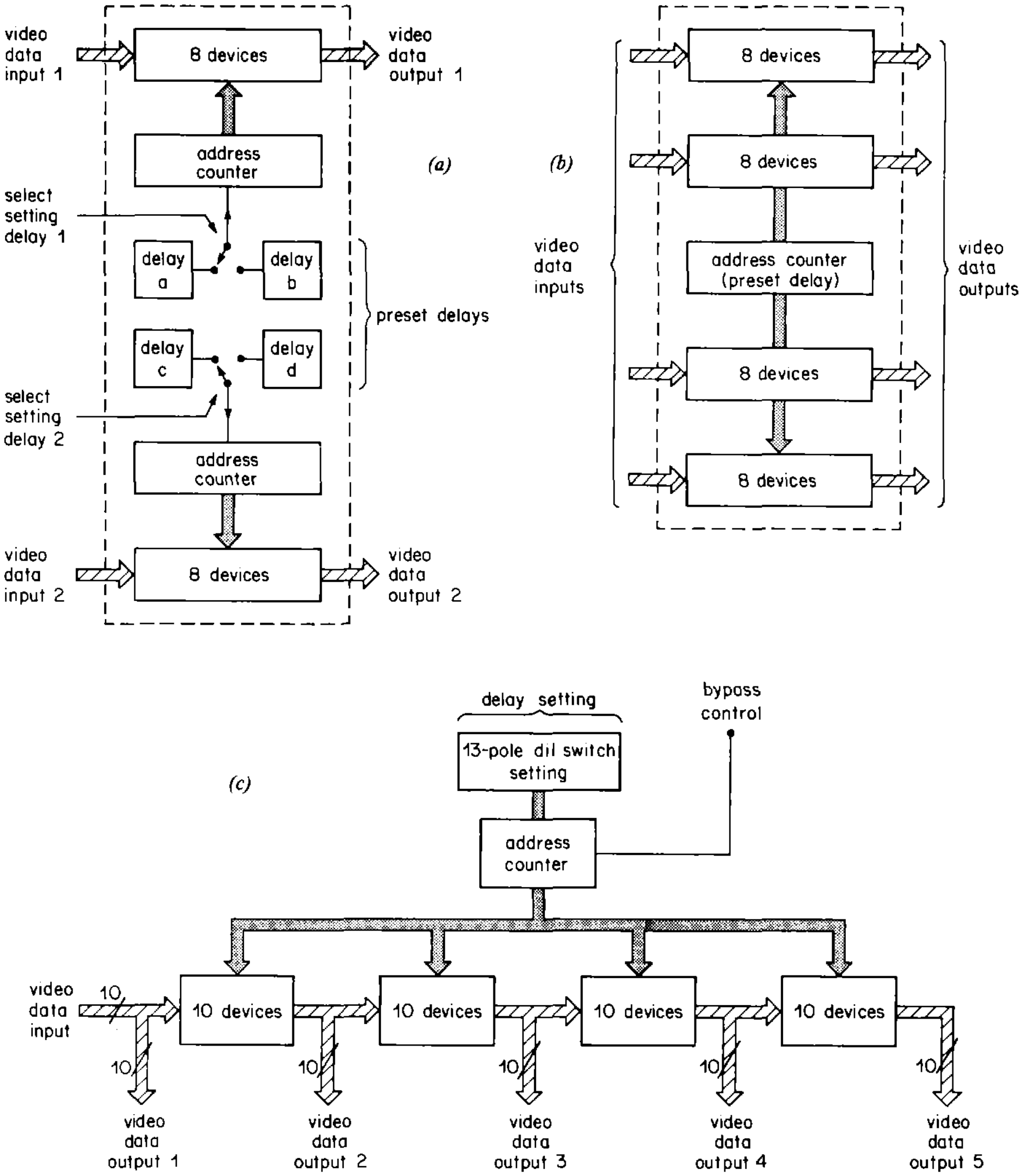

Fig. 25 - Television line delay arrangements. (a) dual line delay with independent control
(b) quadruple line delay with common control (c) quadruple two-line delay with common control

chips to match video data rates. The full standard television *RGB* data rate of 324 Mbit/s is easily obtained by adding extra store boards. Full-size HDTV pictures can be accommodated by accessing further stores in parallel. There is no restriction on the phasing of the store cycle making it possible to lock easily to an external source of mixed synchronising pulses. A 'clean' environment is not essential. Another advantage is that a bulk store based on semiconductor memory chips can be built in several units, each of which is useful in its own right and can be operated by several users independently. One unit could be

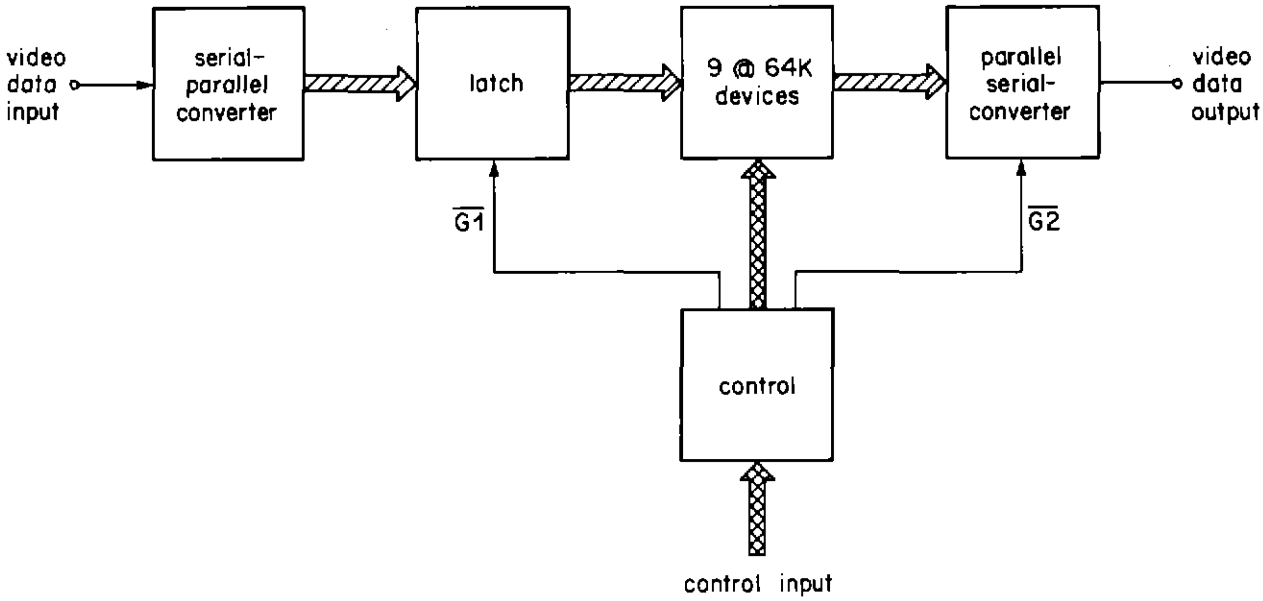

Fig. 26 - Block diagram of a programmable picture delay.

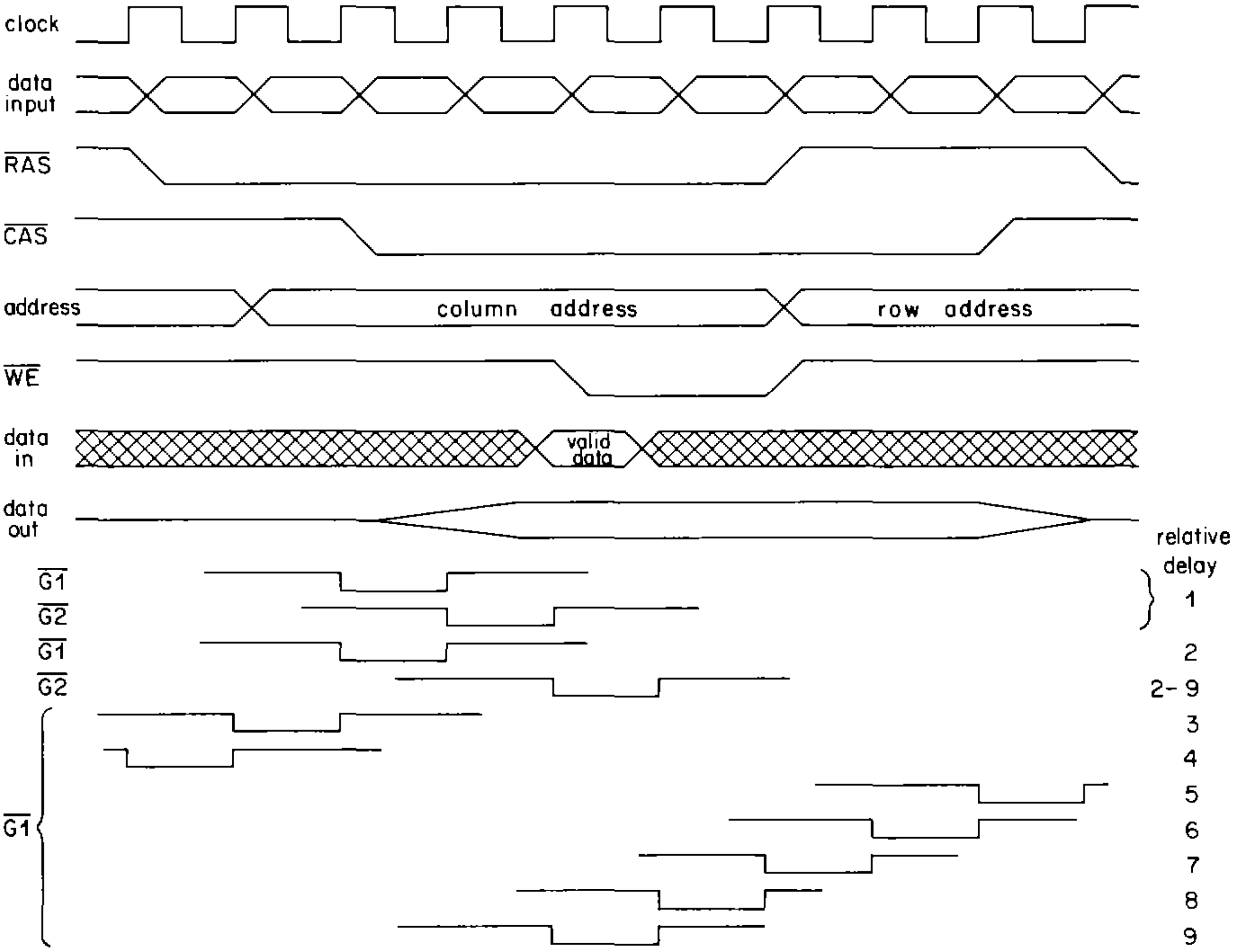

Fig. 27 - Signal waveforms associated with a programmable picture delay.

built initially with relatively little capital outlay and the individual store boards of a unit are interchangeable.

There are three main disadvantages. The first is that the memory must be pre-loaded, at power-on, from a back-up device — for example, a streaming tape cartridge or, for faster operation, a Winchester disk. Secondly, dynamic memory chips require frequent 'refreshing' to maintain their memory. If accidental power loss is to be safeguarded, special provision must be made to generate sufficient refresh cycles to allow the memory to be backed up immediately. This may require some form of battery facility. Thirdly, the length of picture sequence which can be housed in a standard bay is probably limited to about five or six seconds of *RGB* full rate. Longer sequences can only be achieved by reducing the data rate to, say quarter-picture size only or one component only — or by building more bays of equipment.

The remainder of this Section outlines some of the design considerations when using semiconductor memory chips in this application and discusses the specification of a 'package' of storage which can be fabricated on a single p.c.b.

6.2 Choice of memory devices

The 256 K generation of dynamic memory devices is available with a normal minimum read or write cycle time of 200 ns — which is somewhat faster than the 64 K device. A memory cycle of four clock periods at the 13.5 MHz sampling rate (296 ns) is still appropriate, however, and allows the slower versions of the device, which are generally cheaper, to be used with comfortable operating margins and to operate at less than their stated maximum current. To permit simultaneous video read and write or computer read or write at a slower rate, the store must be accessed twice which results in an eight-way demultiplex and a store cycle similar to that used for the 64 K device implementation described in Section 4.2.3. With 256 K devices, therefore, the smallest store possible is 8 x 256 K = 2 Mbit made from eight chips — this is equivalent to four (1 bit) active television pictures.

Another device, for which preliminary data is now available is configured as 32 K x 8 bit. The addressing is direct (15 bit) which results in a faster cycle time of 180 ns minimum and a saving of power —the maximum active current consumption is 55 mA. The byte-wide data bus is shared for input and output data and the device is available either in a 28-pin DIL package (which is relatively large) or a leadless chip carrier which occupies a board area of about 70 mm^2. The same arguments as described above, for multiplexing chips to match video data rates, apply here but there is the possibility of reducing the memory cycle time to three video clock periods (222 ns). This would allow the video demultiplex factor to be decreased to six (for the same dual-port access) or increased to nine to achieve a triple-port access. In the former case it would be necessary to provide more memory addresses than the equivalent store based on a multiplex factor of eight. It may, however, be possible to reduce the total number of a chips required to store a convenient number of active television pictures on a single store board. The faster cycle rate is likely to result in a greater power consumption and decreased operating margin. In the latter case it would be possible conveniently to store four full television pictures in 72 chips but with the same power consumption and operating margin penalties although it is not generally necessary to store the full field and line blanking periods for picture processing purposes.

A 64 K x 4 version is available in an 18-pin DIL package and with similar performance to the 256 K x 1. This device makes it possible to upgrade the compact picture store board described in Section 4.2.2 and quadruple its storage to four pictures with 4-bit per board.

6.3 Store board organisation

There have been previous attempts to make general memory storage boards so that individual users can match them to their requirements by adding dedicated boards of their own. Experience gained from these attempts, leads to two particular conclusions. The first is that the video demultiplexing of memory chips is best performed on the same board as the chips themselves to avoid carrying an excessive number of data connections from one board to another. Secondly, the memory board should not be too large physically — large board area can result in signal waveform distortions when signals are conveyed from one side of a board to another and this is particularly critical in the case of distributing the video sampling clock.

A reasonable package of memory storage is, therefore, one which can group an array of memory chips with the required video multiplexing and demultiplexing and computer decoding chips on a board which is not too large. A greater physical package efficiency may be achieved by moving from 4U memory boards to 6U. A 4U board is capable of supporting 32 memory chips comfortably (the compact *RGB* picture store memory board is an example of this): it may be possible to support 64 memory chips on a board only 50% larger because there is very little increase in the number of ancillary chips needed to support them. This hypothesis forms the basis of a new memory store board design which has both video read and video write ports as well as a computer data port and has a capacity of 4 Mnibble (4 bits wide).

6.4 A rack of storage and beyond

An arrangement of 24 such boards, grouped in pairs suitable for mounting in a single rack of hardware is shown in the block schematic of Fig. 28. They are configured in this case as eight boards each for *RGB* making a total storage capacity per rack of almost 50 Mbyte. The video input processing required to strip off line codes and to interface video to the store boards can be handled on one board. Similarly video output processing requires one board to apply video blanking and re-insert the line codes. A clock pulse generator, capable of being locked to supplied mixed synchronising pulses, provides an internal source of clocks. Alternatively clocks may be provided from video input data. Each store board requires a 21-bit address (15 for each chip and 6 to distinguish 1 of 64 chips) and two further bits are required in each rack to distinguish one of four boards for *RGB* — this makes a total of 23 address bits. This, together with the usual memory control signals, is generated on a separate control board.

An image-processing tool incorporating a large television picture sequence store is presented in the block diagram of Fig. 29. Based on a commercial 16-bit microcomputer, it incorporates a Winchester disk and streaming tape drive for picture back-up and an interface to a fast local area network (LAN) for interconnection to a more powerful processor, for example, a VAX 11/750. The sequence store may be used for:

a) the random access of the data associated with individual pictures, part pictures or pixels within a picture.

b) the output of a sequence of pictures at video rate. One bay would provide about 5 seconds of *RGB* active picture area. Alternatively the addressing could be arranged to give, say, an *RGB* quarter-picture area sequence for 20 seconds or a single component (*Y*) sequence, quarter-picture area for one minute.

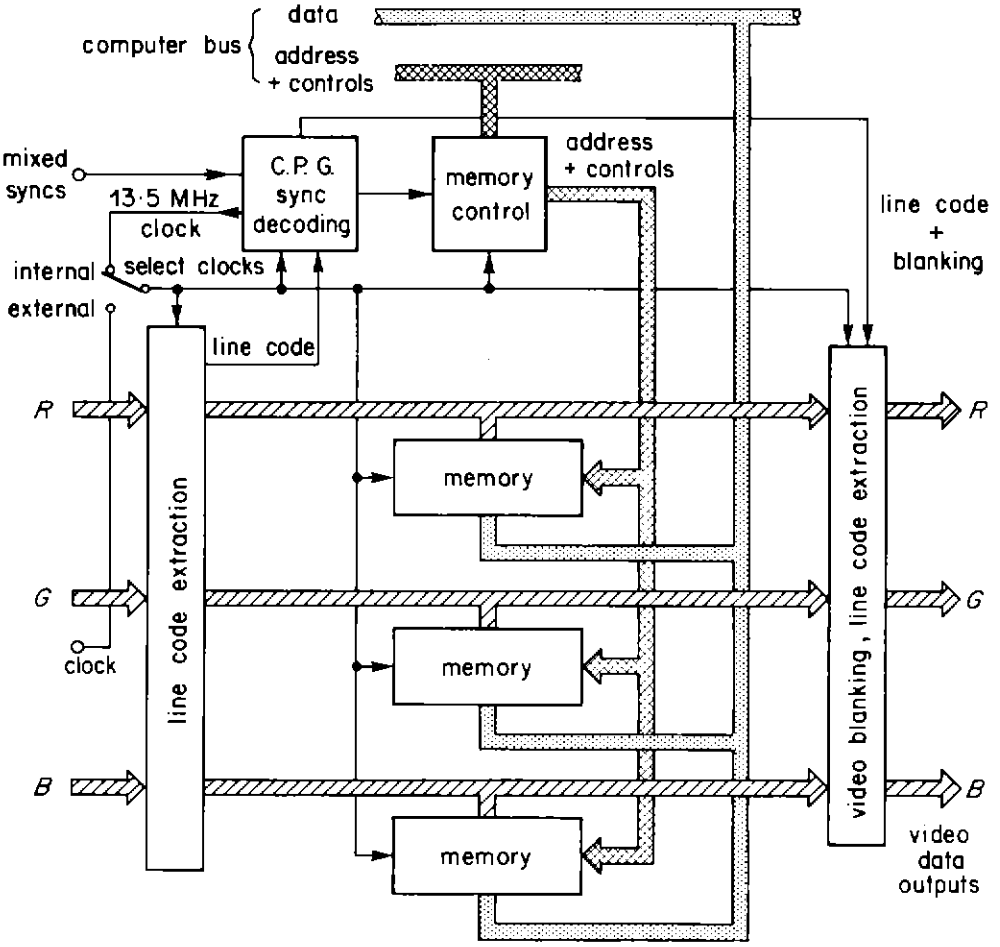

Fig. 28 - Block diagram of a 50 Mbyte store module arranged for RGB data.

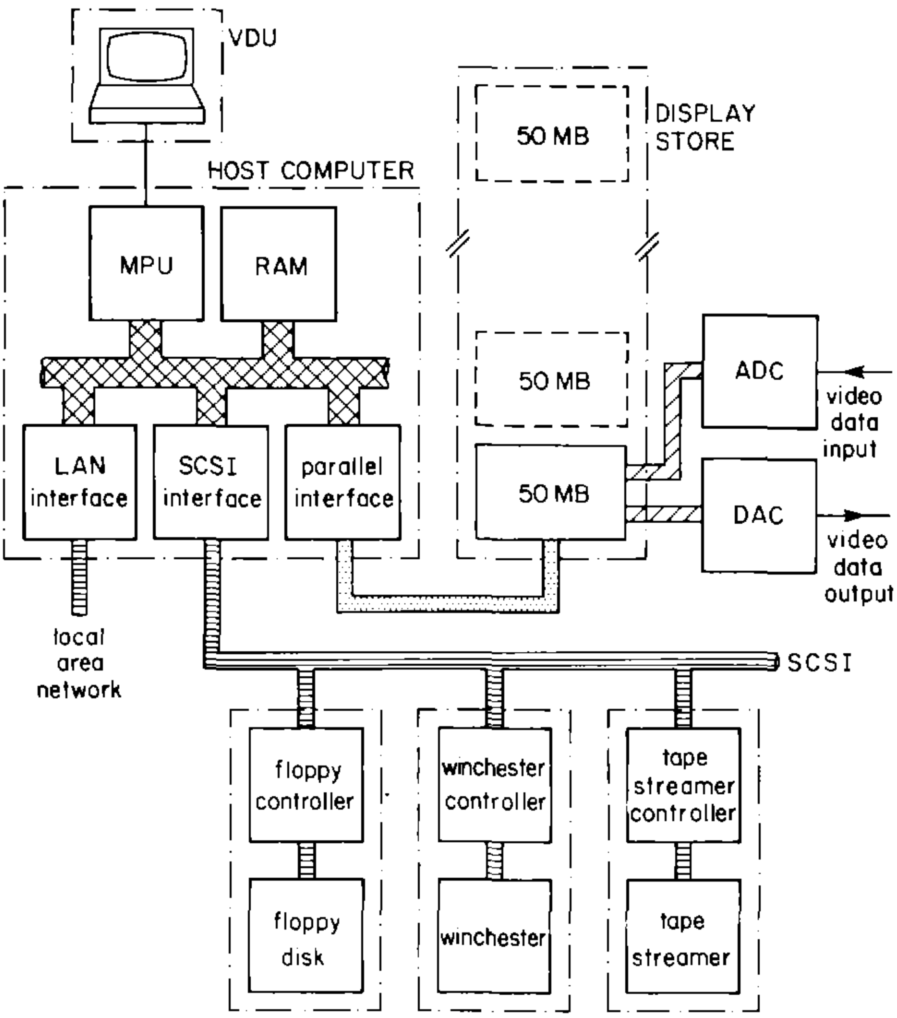

Fig. 29 - An image-processing tool incorporating a television picture sequence store.

7. FUTURE OUTLOOK

As the delay-power product improves and the cost per bit falls there will be a tendency towards the inclusion of a greater amount of storage in professional equipment. This could take the form of digital filters with improved performance, employing picture and field delay taps, for example, to achieve a sophisticated PAL decoder which makes a better job of separating the chrominance and luminance information from a composite signal. Greater mass storage could herald stills stores of even greater capacity, capable of holding the equivalent of hundreds of digital television pictures for almost instant retrieval and display.

The technology trend also brings improvements to the domestic consumer. We can expect improved PAL decoders to find their way into television sets for improved picture quality at little extra cost. Further improvements in picture quality may be achieved by conversion to a better display standard with a higher field rate to reduce picture flicker. Moreover, current proposals for a High Definition Television (HDTV) standard and its practical transmission using Digitally Assisted Television (DATV) signals depend upon the provision of greater intelligence and several television fields of storage within the receiver.

In teletext, a potentially greater storage capacity promises multi-page and fast access, eventually reaching a stage where a whole magazine can be downloaded and stored within the receiver in a single transmission cycle. Also, there is the possibility of including high-quality picture inserts within teletext transmissions.

8. CONCLUSIONS

In this, the second of two Reports, specific applications of semiconductor technology to the design of equipment which can store television signals in digital form have been described and discussed. All the items were developed at BBC Research Department during the last decade and have been or still are in regular use in the BBC Television Service.

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